TEST MAINTENANCE
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OPERATION AND MAINTENANCE MANUAL DIFAR SYSTEM SIMULATOR CD 3800

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BROWN ENGINEERING

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OPERATION AND MAINTENANCE

MANUAL

DIFAR SYSTEM SIMULATOR

SPECIFICATION DS 3800

PART NUMBER CD 3800

ISSUED:

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INTRODUCTION

SCOPE OF MANUAL:

This manual is intended to provide operating and maintenance personnel with sufficient technical information to permit correct use and maintenance of the DIFAR System Simulator.

PURPOSE OF SIMULATOR:

The DIFAR System Simulator is designed to generate the controlled active and passive sonic signals necessary to conduct the acceptance tests on the AN/AQA-7(V) Aircraft Data Processor System.

1.0 INSTALLATION:

The DIFAR System Simulator will be installed under the direction of the Brown Engineering Resident Engineer. All questions pertaining to installation or checkout immediately after installation should be directed to him.

2.0 SYSTEM DESCRIPTION:

2.1 MECHANICAL:

The DIFAR System Simulator generates the controlled active and passive sonic signals for conducting the acceptance test on the AN/AQA-7(V) Aircraft Data Processor System. The system is housed in standard 19-inch relay racks. The main chassis is mounted on casters which have locking mechanisms. The system is shown in Figure 2-1. The top unit is the AC Power Panel which supplies filtered AC to the system. The second and fourth panels are blank. The third unit is the Control Panel, which contains all of the electronic circuits necessary to simulate the DIFAR System. DC power for the Control Panel is supplied by the Power Supply Panel located below the Control Panel. The blower, located at the bottom of the rack, provides cooling air. A writing surface is provided immediately below the Control Panel. The rack contains a rear door which allows access to the back of the Power Supply Panel, the Control Panel Assembly and the AC Power Control Panel. Connection to the system under test is made through three receptacles located on the rack behind the blower section.

The AC Power Panel is located at the top of the DIFAR System Simulator. The panel consists of an elapsed time indicator (ETI) for recording system operating time, a power on light and a double circuit breaker which serves as the system on-off

FIGURE 2-1. DIFAR SYSTEM SIMULATOR CD-3800

switch. AC power, 115 volt, 60 cycle single phase, enters through a Arrow Hubble #7323 recessed male plug located on the top of the rack. It is filtered prior to being routed to the circuit breaker in the AC Power Control Panel. AC power is distributed to the system units from the circuit breaker through a plug mold in the rack.

The Control Panel is the heart of the Simulator. This unit contains all of the circuitry necessary, except power supplies, to generate the outputs required. It consists of the front panel controls, the recessed panel controls, 57 printed circuit cards with provisions for three additional cards, and a track bearing generator module. The Control Panel is mounted on equipment slides to allow extension of the unit for calibration or maintenance. This is accomplished by loosening the four thumb screws located in each corner of the front panel and pulling on the handles provided.

The Power Supply Panel provides the DC power necessary for the Control Panel. It consists of six individual power supply modules and a voltage doubler. The power supply modules are individually adjustable to the required level: ± 15 volts, +5 volts, +24 volts. The Power Supply Panel is also mounted on equipment slides.

The Blower is a 415 cfm, Amco P/N B400 rack mounted blower. The intake air is through a filter located at the front of the blower. The exhaust air exits through the perforated top cover of the rack providing cooling air for all units. The blower allows the system to operate in an ambient temperature up to +95°F.

2.2 SYSTEM SPECIFICATIONS:

2.2.1 Electrical:

AC Power: 115 ±10 volts, 60 ±2 Hz.

Warm Up Time: 30 minutes

Input Signals: see Table 2-1

Output Signals: see Table 2-1

Operating Life: 5 years

2.2.2 Mechanical:

Height: 72.56 inches (with casters)

70.00 inches (rack only)

Width: 23.44 inches

Depth: 28.38 inches

2.2.3 Environmental:

Operating Temperature Range: $+65^{o}F$ to $+95^{o}F$

room ambient

Humidity: up to 95 percent relative

Vibration and Shock: 3g

TABLE 2-1

DIFAR SYSTEM SIMULATOR
INPUTS AND OUTPUTS

J2 - INPUT/OUTPUT CONNECTOR

PIN	FUNCTION	
F	$\overline{t_0}$ Test	
G	Remote TRACK Input-OMNI	Hi
H	Remote TRACK Input-OMNI	Lo
J	Remote TRACK Input-OMNI	Shield
K	Remote TRACK Input-NS	Hi
L	Remote TRACK Input-NS	Lo
M	Remote TRACK Input-NS	Shield
N	Remote TRACK Input-EW	Hi
P	Remote TRACK Input-EW	Lo
R	Remote TRACK Input-EW	Shield
S	BITE ASSG Output	Hi
T	BITE ASSG Output	Lo
U	BITE ASSG Output	Shield
V	BITE ASSG Relay Coil	
W	Relay Power	
X	Simulator Logic Ground	
Y	Simulator Chassis Ground	
Z	DIFAR I	Hi
a	DIFAR I	Lo
b	DIFAR I	Shield
c	DIFAR II	Hi
d	DIFAR II	Lo
e	DIFAR II	Shield
f	DIFAR III	Hi
g	DIFAR III	Lo
h	DIFAR III	Shield
i	DIFAR IV	Hi
j	DIFAR IV	Lo
k	DIFAR IV	Shield

TABLE 2-1 (continued)

J2 (continued)

PIN	FUNCTION	
m	OMNI Search A	Hi
n	OMNI Search A	Lo
p	OMNI Search A	Shield
q	OMNI Search B	Hi
r	OMNI Search B	Lo
s	OMNI Search B	Shield
t	OMNI Search C	Hi
u	OMNI Search C	Lo
v	OMNI Search C	Shield
w	OMNI Search D	Hi
x	OMNI Search D	Lo
y	OMNI Search D	Shield
z	Active Ranging Audio Range A	Hi
AA	Active Ranging Audio Range A	Lo
BB	Active Ranging Audio Range A	Shield
CC	Active Ranging Audio Range B	Hi
DD	Active Ranging Audio Range B	Lo
EE	Active Ranging Audio Range B	Shield
FF	Active Ranging Gate Range A	Hi
GG	Active Ranging Gate Range A	Lo
HH	Active Ranging Gate Range A	Shield
JJ	Active Ranging Gate Range B	Hi
KK	Active Ranging Gate Range B	Lo
LL	Active Ranging Gate Range B	Shield
MM	ASSG Input	Hi
NN	ASSG Input	Lo
PP	ASSG Input	Shield

TABLE 2-1 (continued)

J1 - INPUT/OUTPUT CONNECTOR

PIN	FUNCTION	
X	Range Select	Hi
Y	Range Select	Lo
Z	Range Select	Shield
a	Q50 0.1	Hi
b	Q50 0.1	Lo
c	Q50 0.1	Shield
d	Q50 0.5	Hi
e	Q50 0.5	Lo
f	Q50 0.5	Shield
g	Q50 1.0	Hi
h	Q50 1.0	Lo
i	Q50 1.0	Shield
j	FM UP	Lo
k	FM UP	Hi
m	FM UP	Shield
n	FM DOWN	Hi
p	FM DOWN	Lo
q	FM DOWN	Shield
r	Manual Ping A	Hi
s	Manual Ping A	Lo
t	Manual Ping A	Shield
u	Manual Ping B	Hi
v	Manual Ping B	Lo
w	Manual Ping B	Shield
x	Simulator Logic Ground	
y	Simulator Chassis Ground	
z	External Print Drive Units Digit Binary 1	
AA	External Print Drive Units Digit Binary 2	
BB	External Print Drive Units Digit Binary 4	

TABLE 2-1 (continued)

J1 (continued)

PIN	FUNCTION
CC	External Print Drive Units Digit Binary 8
DD	External Print Drive Tens Digit Binary 1
EE	External Print Drive Tens Digit Binary 2
FF	External Print Drive Tens Digit Binary 4
GG	External Print Drive Tens Digit Binary 8
HH	External Print Drive Hundreds Digit Binary 1
JJ	External Print Drive Hundreds Digit Binary 2
KK	External Read Alarm
LL	External Print Command
MM	Track Signal Ground
NN	Simulator Logic Ground
PP	Simulator Chassis Ground

P3 - GROUND CONNECTOR

PIN	FUNCTION
Single Pin Ground Connector	Simulator Chassis Ground

3.0 OPERATING INSTRUCTIONS:

Operation of the DIFAR System Simulator is always in conjunction with a Magnavox test procedure. Therefore, the purpose of this section is only to acquaint the user with the function of each control and to explain how to set up the system for each mode of operation.

3.1 CONTROLS:

The majority of controls for the DIFAR System Simulator are located on the front panels of the Control Panel and AC Power Panel. Table 3-1 provides a list of the controls and the functions performed. The controls located on the recessed panel of the Control Panel assembly are used only during internal control (LOCAL) of the Active Mode. The normal setup will be for remote control of the Active Mode by the AN/AQA-7(V).

In addition to the front panel controls, a switch panel is located inside the Control Panel. These switches are used during calibration, maintenance, and checkout of the system. The functions of each switch are shown in Table 3-2.

The following section provides the procedures for operating the Simulator. These instructions assume the system has been properly installed and connected to an AC power source.

TABLE 3-1

FRONT PANEL CONTROLS

Switch Number	Title	Positions	Function
	CONTROL PANEL		
	PASSIVE MODE		
S1	BITE Control	NORM SS 1/2 NORM SS 6 EXT SS 1/2 EXT SS 6 DL	Selects the BITE signal condition.
S2	Mode	BITE LOFAR ALI LOFAR DIFAR DEMON TRACK DL ASSG	Selects signal to the four DIFAR and four OMNI Search outputs.
S3	DL Bearing	0°, 45°, 90°, 135°, 180°, 225°, 270°, 315°	Selects target bearing in DL position of Mode switch.
S4	S/N Level	1 2 3	Selects signal-to-noise ratio in DIFAR and DL modes.
S5 S6 S7 S8	DIFAR Outputs GRAM I GRAM II GRAM III GRAM IV	SIMULATOR BITE	Selects either the normal output as defined by the Mode switch, or the BITE output signal.
S9 S10 S11 S12	Omni Search Outputs TRACE A TRACE B TRACE C TRACE D	SIMULATOR BITE	Selects either the normal output as defined by the Mode switch, or the BITE output signal.
S13	Bandwidth	NORM EXT	Selects target frequency band.

TABLE 3-1

FRONT PANEL CONTROLS
(continued)

Switch Number	Title	Positions	Function
	CONTROL PANEL (cont.)		
	PASSIVE MODE (cont.)		
S14	Crosstalk	ON OFF	Applies strong signal-to-noise on LOFAR, ALI LOFAR, or DIFAR signals and inhibits BITE targets.
DS1	AC Power	ON OFF	Illuminated-AC Power ON Dark-AC Power OFF.
F-1	Fuse		Fuses AC Power to Control Panel (target bearing generator motor).
DS2	Tracking Degrees	--	3-digit decade readout indicates internally generated TRACK signal bearing angle in degrees.
DS3	6° Alarm	--	Panel light illuminates each 6 degrees advance of internally generated TRACK signal bearing angle.
	ACTIVE MODE		
S15	Ping Frequency	26 KHz 38 KHz	Selects ping frequency for Q-47.
S16	Zero Doppler	750 Hz 950 Hz	Selects zero doppler frequency for Q-47.
S17	Ping	A and B A or B	Permits both Range A and B to be controlled either together, or independently.

TABLE 3-1

FRONT PANEL CONTROLS
(continued)

Switch Number	Title	Positions	Function
	CONTROL PANEL (cont.)		
	ACTIVE MODE (cont.)		
S18	B Ping	ZERO DELAY DELAYED 6K YARDS	Provides Range B ping either coincidentally with Range A or 8 seconds after Range A.
S19	Range A	Signal + Noise Noise Only	
S20	Range B	Signal + Noise Noise Only	
	TEST		
S21	Active Mode Control	LOCAL REMOTE	Selects either external or internal control of the active mode.
S22	Ping Control	AUTO MANUAL	AUTO: Range A pinged automatically every 16 seconds independent of Active Mode Control switch setting. MANUAL: Permits manual ping of Range A or B according to position of Active Mode Control switch
S23	Track Bearing	LOCAL REMOTE	LOCAL: Selects internally generated TRACK output in TRACK position of Mode switch. REMOTE: Selects Remote Track Inputs in TRACK position of Mode Switch for externally controlled bearing signal generation.

TABLE 3-1

FRONT PANEL CONTROLS
(continued)

Switch Number	Title	Positions	Function
	CONTROL PANEL (cont.)		
	TEST (cont.)		
J1	Remote Track Bearing Input	--	Provides input jack for external track bearing signal.
S24	Oscillator Test	OFF or Position 1 through 35	Selects oscillator frequency available at oscillator test jack.
J2	Oscillator Output	--	Oscillator output test jack.
	RECESSED PANEL		
	ACTIVE		
S25	Ping Width	0.1 (seconds) 0.5 1.0	Selects ping width in Q50 CW mode.
S26	CASS	CW FM	Selects CW or FM submode of Q50.
S27	FM	UP DOWN	Selects UP or DOWN FM output ramp.
S28	BUOY	Q47 Q50	Local sonobuoy control: Q47 or Q50 mode selection.
S29	Range A	--	Depress to initiate Range A manual ping.
S30	Range B	--	Depress to initiate Range B manual ping.

TABLE 3-1

FRONT PANEL CONTROLS
(continued)

Switch Number	Title	Positions	Function
AC POWER CONTROL PANEL			
I1	AC Power		Illuminated-AC Power ON Dark-AC Power OFF.
ET11	Elapsed Time		Equipment elapsed running time.
S1	Main Power	OFF ON	Master circuit breaker.

TABLE 3-2

INTERNAL SWITCH PANEL

Switch Number	Title	Positions	Function
INTERNAL SWITCH PANEL			
S31	OSC	OFF	Inhibits Oscillator Outputs
		ON	Permits Oscillator Outputs
S32	NOISE	OFF	Inhibits Noise
		ON	Permits Noise
S33	NS	OFF	Inhibits NS Modulator
		ON	Permits NS Sidebands
S34	EW	OFF	Inhibits EW Modulator
		ON	Permits EW Sidebands
S35	15	OFF	Inhibits 15 KHz Pilot
		ON	Permits 15 KHz Pilot
S36	7.5	OFF	Inhibits 7.5 KHz Pilot
		ON	Permits 7.5 KHz Pilot
S37	OMNI	OFF	Inhibits Omni Noise
		ON	Permits Omni Noise
S38	PLT	OFF	Inhibits BITE 7.5 KHz and 15 KHz Pilots
		ON	Permits BITE Pilots
S39	117/234	OFF	Inhibits 117/234 BITE Output
		ON	Permits 117/234 BITE Output
S40	MT	OFF	Inhibits BITE MT
		ON	Permits BITE MT

3.2 INITIAL SETUP:

The DIFAR System Simulator requires a thirty-minute warm-up period. During this thirty minutes, the system can be set up for operation. The Simulator operates in PASSIVE AND ACTIVE modes simultaneously; the following instructions are broken out into PASSIVE and ACTIVE only to simplify the procedures. The Simulator will always be operated in conjunction with a Magnavox test procedure; the options available on the switch settings will be determined by those procedures.

3.3 PASSIVE MODE:

3.3.1 General:

Step A: Set S24 to OFF.

Step B: Set S31 through S40 to ON (inside of Control Panel).

Step C: Set the S2 mode switch to <u>any position except</u> TRACK. In the TRACK mode, the target bearing generator operates. Once the motor starts, it takes one hour to complete one revolution; it cannot be reset to ZERO.

Step D: Turn the AC power ON (S1 of the AC Power Panel).

Step E: Set S14 to OFF.

3.3.2 BITE Mode:

Step 1: Perform steps A through E of PASSIVE Mode General.

Step 2: Set S2 to BITE.

Step 3: Set S1 to desired band and signal level:

a. NORM SS 1/2 = NORMAL target frequency band, level 1 signal.

b. NORM SS 6 = NORMAL target frequency band, level 3 signal.

c. EXT SS 1/2 = EXTENDED target frequency band, level 1 signal.

d. EXT SS 6 = EXTENDED target frequency band, level 3 signal.

e. DL - BITE circuits DL Mode.

Step 4: Set switches S5 through S12 to BITE.

The position of the remaining switches will not have any effect on BITE mode of operation.

3.3.3 LOFAR Mode:

Step 1: Perform steps A through E of PASSIVE Mode General.

Step 2: Set S2 to LOFAR.

Step 3: Set S5 through S12 to Simulator GRAM I through GRAM IV and TRACE A through TRACE D respectively.

Step 4: a. Set S13 to NORM for normal target frequency band.

b. Set S13 to EXT to extended target frequency band.

The position of the remaining switches will not have any effect on the LOFAR mode of operation.

3.3.4 ALI LOFAR Mode:

Step 1: Perform steps A through E of PASSIVE Mode General.

Step 2: Set S2 to ALI LOFAR.

Step 3: Set S5 through S8 to Simulator GRAM I through GRAM IV respectively.

Step 4: Set S9 through S12 to Simulator TRACE A through TRACE D respectively.

Step 5: a. Set S13 to NORM for normal target frequency band.

b. Set S13 to EXT for extended target frequency band.

The position of the remaining switches will not have any effect on the ALI LOFAR mode of operation.

3.3.5 DIFAR Mode:

Step 1: Perform steps A through E of PASSIVE Mode General.

Step 2: Set S2 to DIFAR.

Step 3: a. Set S4 to 3 for a level 3 signal.

b. Set S4 to 1 for a level 1 signal.

Step 4: Set S5 through S8 to SIMULATOR GRAM I through GRAM IV respectively.

Step 5: a. Set S13 to NORM for normal target frequency band.

b. Set S13 to EXT for extended target frequency band.

The position of the remaining switches will not have any effect on the DIFAR mode of operation.

3.3.6 DEMON Mode:

Step 1: Perform steps A through E of PASSIVE Mode General.

Step 2: Set S2 to DEMON.

Step 3: Set S5 through S8 to SIMULATOR GRAM I through GRAM IV respectively.

The position of the remaining switches will not have any effect on the DEMON mode of operation.

3.3.7 TRACK Mode:

Step 1: Perform steps A through E of PASSIVE Mode General.

WARNING: Some test procedures require that the TRACKING DEGREES, DS2, reading be 000. Do not set S2 to TRACK until instructed to do so.

Step 2: Set S5 through S8 to SIMULATOR GRAM I through GRAM IV respectively.

Step 3: a. Set S23 to LOCAL for Simulator control.

b. Set S23 to REMOTE for external control (requires input to J1, remote TRACK bearing input).

Step 4: When instructed, set S2 to TRACK.

NOTE: If the DS1 reading is not 000, refer to specific test procedure in effect to determine if this is important. If a 000 reading is necessary, set S2 to TRACK and wait for 000 reading. When it occurs, set S2 to BITE and notify individual in charge of test that the Simulator is ready. Set S2 to TRACK only when test is to begin.

3.3.8 DL Mode:

Step 1: Perform steps A through E of PASSIVE Mode General.

Step 2: Set S2 to DL.

Step 3: Set S3 to 0°, 45°, 90°, 135°, 180°, 225°, 270°, or 315° as directed by the test procedure.

Step 4: a. Set S4 to 1 for a level 1 signal.

b. Set S4 to 2 for a level 2 signal.

c. Set S4 to 3 for a level 3 signal.

Step 5: Set S5 through S8 to SIMULATOR, GRAM I through GRAM IV respectively.

The position of the remaining switches will not have any effect on the DL mode of operation.

3.3.9 ASSG Mode:

Step 1: Perform steps A through E of PASSIVE Mode General.

Step 2: Set S2 to ASSG.

Step 3: Set S5 through S8 to SIMULATOR, GRAM I through GRAM IV respectively.

Step 4: Set S9 through S12 to SIMULATOR, TRACE A through TRACE D respectively.

The position of the remaining switches will not have any effect on the ASSG mode of operation.

3.4 ACTIVE MODE:

Step 1: Set switches S31 through S40 to ON (internal switch panel).

Step 2: Set S24 to OFF.

Step 3: a. Set S21 to REMOTE for external control.

b. Set S21 to LOCAL for internal control.

NOTE: The following switch settings are all dependent on the specific test to be run. Refer to the test procedure in effect to determine what condition is required.

Step 4: a. Set S22 to AUTO for automatic operation.

b. Set S22 to MANUAL for manual ping.

Step 5: a. Set S15 to 26 KHz for a 26 KHz ping frequency.

b. Set S15 to 38 KHz for a 38 KHz ping frequency.

Step 6: a. Set S16 to 750 Hz for a 750 Hz zero doppler.

b. Set S16 to 950 Hz for a 950 Hz zero doppler.

Step 7: a. Set S17 to A or B if only one channel is desired (the specific channel is selected in step 8 below).

b. Set S18 to A and B for output on both channels.

Step 8: a. If S17 was set to A or B and Channel A is desired, set S19 to RANGE A and S20 to NOISE ONLY.

b. If S17 was set to A or B and Channel B is desired, set S19 to NOISE ONLY and S20 to RANGE B.

c. If S17 was set to A and B, set S19 to RANGE A and S20 to RANGE B.

Step 9: If S17 was set to A and B:

a. Set S18 to ZERO DELAY for simultaneous outputs on RANGE A and RANGE B.

b. Set S18 to DELAYED 6K YARDS to delay the RANGE B output until the 6K yard target time is reached.

If S21 was set to REMOTE in step 3, the position of the remaining switches will not affect the ACTIVE mode of operation. If S21 was set to LOCAL in step 3, the following steps must be performed. Again, the options available will be determined from the test procedure in effect.

Step 10: a. Set S27 to Q47 for the Q47 mode of operation. Additional switch settings are not necessary in Q47 mode. Proceed to step 13.

b. Set S28 to Q50 for Q50 mode of operation.

Step 11: a. Set S26 to CW for Q50 CW and proceed to step 12a.

b. Set S26 to FM for Q50 FM and proceed to step 12b.

Step 12: a. Set S25 to 0.1, 0.5, or 1.0 for 0.1, 0.5, or 1.0 second ping width respectively.

b. Set S28 to UP for a FM ramp up. Set S28 to DOWN for a FM ramp down.

Step 13: If in step 8, Range A was selected, depress S29 to start operation. If Range B was selected, depress S30 to start operation. If in step 7, A and B was selected, depress either S29 or S30 to start operation. In manual mode, it is necessary to depress the PING switch to start each cycle.

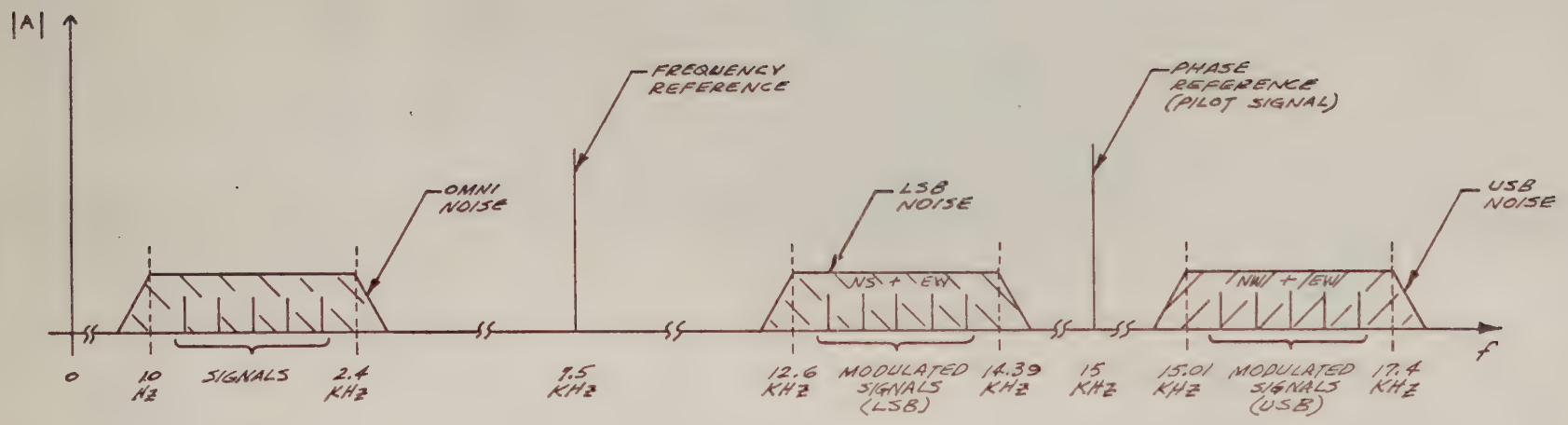
4.0 THEORY OF OPERATION:

The DIFAR System Simulator is a test station that generates the controlled active and passive sonic signals for conducting the acceptance test on the AN/AQA-7(V). The simulator outputs are representative of the signals which are received by the AN/AQA-7(V). There are two basic modes of operation: Passive and Active with several submodes in each. The following paragraphs provide the theory of operation for the system and the detailed theory of operation for the circuits.

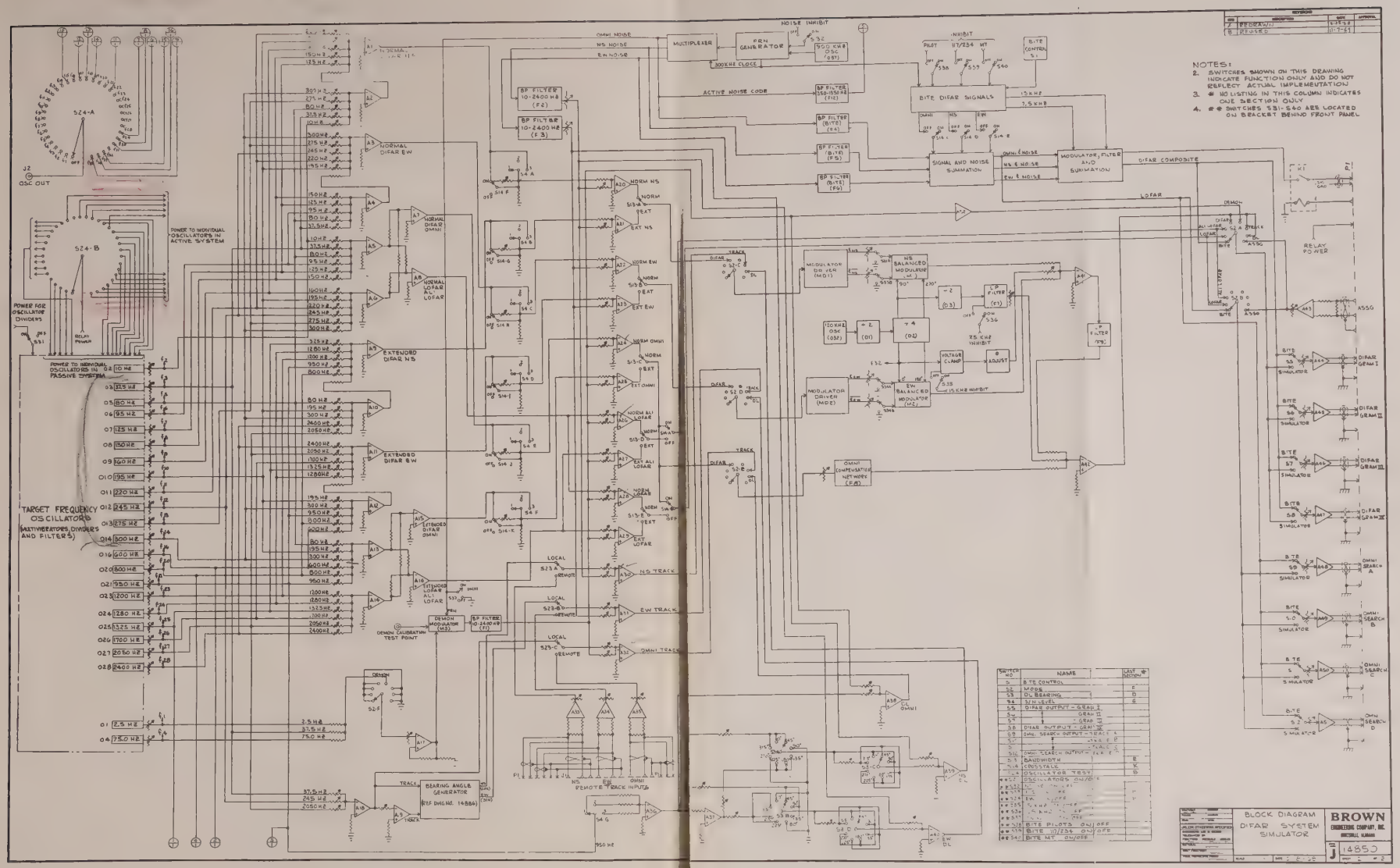
4.1 PASSIVE MODE SYSTEM THEORY:

In the passive mode of operation, the DIFAR System Simulator provides various target frequencies in a noise background. The target frequency sources are oscillators. The noise source is a pseudorandom noise generator (PRN) that operates at a clock frequency of 300K bits per second. The PRN generator outputs are multiplexed into three separate channels providing three uncorrelated outputs.

The passive mode outputs consist of all or part of the waveform shown in Figure 4-1 as determined by the submode. The submodes of operation are LOFAR, ALI LOFAR, DIFAR, DL, TRACK, DEMON, ASSG and BITE. System operation in each mode is described in the following paragraphs. Refer to Figure 4-2 while reading the mode descriptions.



COMPOSITE OUTPUT SIGNAL SPECTRUM
FIGURE 4-1



SWITCH NO.	NAME	LAST # SECTION
S1	BITE CONTROL	
S2	MODE	E
S3	DL BEARING	D
S4	SIN LEVEL	E
S5	DIFAR OUTPUT - GRAM I	
S6	GRAM II	
S7	GRAM III	
S8	DIFAR OUTPUT - GRAM IV	
S9	OMNI SEARCH OUTPUT - SEARCH A	
S10	SEARCH B	
S11	SEARCH C	
S12	OMNI SEARCH OUTPUT - SEARCH D	
S13	BANDWIDTH	E
S14	CONSTALL	E
S15	OSCILLATOR TEST	B
## S16	OSCILLATORS ON/OFF	
## S17	[illegible]	
## S18	[illegible]	
## S19	[illegible]	
## S20	[illegible]	
## S21	[illegible]	
## S22	[illegible]	
## S23	[illegible]	
## S24	[illegible]	
## S25	[illegible]	
## S26	[illegible]	
## S27	[illegible]	
## S28	BITE PILOTS ON/OFF	
## S29	BITE 17/234 ON/OFF	
## S30	BITE MT ON/OFF	

FIGURE 4-2. PASSIVE MODE FUNCTIONAL BLOCK DIAGRAM

4.1.1 LOFAR Mode:

The LOFAR mode provides only the omni portion of the waveform of Figure 4-1. It consists of multitargets in a level 1 noise background. The target frequencies can be either the normal band or extended band shown in Table 4-1. The extended or normal band is a front panel selection, S13.

When LOFAR is selected on S2, the required oscillator outputs are gated to a linear summing amplifier A8 (normal) or A16 (extended) whose output is sent to a signal/noise summing amplifier A28 (normal) or A29 (extended). The output of the signal/noise summing amplifier is applied to the four DIFAR output amplifiers, A44 through A47, and the OMNI Search amplifiers, A48 through A51, through the mode switching circuits.

4.1.2 ALI LOFAR Mode:

System operation in ALI LOFAR mode is identical to LOFAR except that the signal noise ratio requirements are different. The signal-to-noise ratio is established by the input resistors of the signal/noise summing amplifiers A26 (normal) or A27 (extended). The target frequencies are shown in Table 4-1.

TABLE 4-1

MODE TARGET FREQUENCIES

TARGET FREQUENCY (Hz)	LOFAR		ALI LOFAR		DIFAR		TRACK (Note 1)	DL (Note 2)
	NORM	EXT	NORM	EXT	NORM	EXT		
10	X		X		X			
37.5	X		X		X		X	
80	X	X	X	X	X	X		
95	X		X		X			
125	X		X		X			
150	X		X		X			
160	X		X		X			
195	X	X	X	X	X	X		
220	X		X		X			
245	X		X		X		X	
275	X		X		X			
300	X	X	X	X	X	X		
600		X		X		X		
800		X		X		X		
950		X		X		X		X
1200		X		X		X		
1280		X		X		X		
1325		X		X		X		
1700		X		X		X		
2050		X		X		X	X	
2400		X		X		X		

Note 1: Targets occur at continuously changing bearing.

Note 2: Target occurs at 0°, 45°, 90°, 135°, 180°, 225°, 270°, or 315°.

4.1.3 DIFAR Mode:

The DIFAR mode outputs consist of the entire waveform shown in Figure 4-1. The target frequencies can be either the normal or extended band shown in Table 4-1. These target frequencies occur at various, fixed bearings in the NS and EW sidebands of the 15 kHz pilot. The bearings are simulated by varying the target signal amplitude. The following description will cover only the normal band.

The required target frequencies are sent to signal summing amplifiers A7, A1, and A3 (A2, A4, A5, and A6 provide expansion abilities for A1, A3, and A7). The A7 amplifier is the omni portion of the output (see Figure 4-1). Its output passes through switch S4E for a level 3 signal or through a resistor for a level 1 signal. The DIFAR omni signal then enters amplifier A24 where it is combined with the noise. The A24 output is fed through F8, omni compensation network to summing amplifier A42. F8 is a network which shifts the phase of the omni signal to compensate for the phase shift which occurs on the rest of the waveform in the modulator.

The output of the A1 amplifier passes through S4A or a resistor to establish the signal level, then to A20 amplifier where it is summed with noise. This composite is then sent to the NS side

of a dual balanced modulator. The A3 output passes through S4C or a resistor to establish the signal level, then to A22 where it is combined with noise. The A22 output is then sent to the EW position of the dual balanced modulator.

The purpose of the dual balanced modulator is to provide the 7.5 kHz pilot, the 15 kHz pilot, and the EW and NS sidebands of the composite signal shown in Figure 4-1. The 7.5 kHz and 15 kHz pilots must be frequency locked and contain very low distortion.

The 15 kHz pilot originates from a 120 kHz oscillator which is divided by two by D1. The 60 kHz output of D1 is then divided by four by D2. D2 provides four 15 kHz signals at 0°, 90°, 180°, and 270°. The 90° and 270° 15 kHz carriers are supplied to NS balanced modulator M1. This device modulates the 15 kHz carriers with the E_{NS} and $\overline{E}_{NS}$ outputs of modulator driver MD1 (E_{NS} and $\overline{E}_{NS}$ originate from the A20 output). After modulating, the original E_{NS} and $\overline{E}_{NS}$ modulating signal and the 15 kHz (90° and 270°) carriers are balanced out. The output of M1 consists of only the sidebands generated internally. The EW signal is processed in the same manner by MD2 and M2. The four sidebands generated by M1 and M2 are then sent to amplifier A41 where they are summed with the original 15 kHz 0° pilot.

The A41 output is filtered by F9 to attenuate any harmonics and is applied to A42. The 15 kHz 90° pilot is divided by two by D3 to achieve the 7.5 kHz pilot which is also sent to A42. The output of A42 consists of the entire composite shown in Figure 4-1. This signal is sent to the four DIFAR output amplifiers, A44 through A47.

4.1.4 DL Mode:

The DL mode is provided to simulate a single target frequency, 950 Hz, at three different signal levels and selectable bearings. The output consists of the waveform shown in Figure 4-1, but contains only the 950 Hz target in the omni and sideband noise bands.

The 950 Hz oscillator output is passed through one of three weighting resistors to establish the signal level prior to amplification by A36. The A36 output is fed to the signal/noise summing amplifier A38 whose output is passed through omni compensation network, F8, to summing amplifier A42.

The A36 output is also sent to a switching and weighting network represented by A37 and S3. This network establishes the amplitude of the 950 Hz signal to represent the bearing selected by S3. The output of this network is sent to signal/noise summing

amplifier A39 and/or A40, depending on the bearing. These amplifier outputs are inputs for the dual balanced modulator. The DL signal is processed in the same manner in the modulator as the DIFAR signals described above. The result is the 15 kHz pilot with sidebands sent to amplifier A42 where it is joined with the 7.5 kHz pilot and the omni portion of the signal. The output of summing amplifier A42 is then sent to the four output amplifiers A44 through A47.

4.1.5 TRACK Mode:

The TRACK mode is furnished to represent three target frequencies with continuously changing bearings. The output consists of the waveform shown in Figure 4-1.

The outputs of the 37.5 Hz, 245 Hz, and 2050 Hz oscillators are fed into summing amplifier A18. The A18 output is sent directly to signal/noise summing amplifier A32 to develop the omni portion of the waveform. The A32 output is routed through the omni compensation network, F8, to the dual balanced modulator output summing amplifier A42.

The output of A18 is also fed to the target bearing angle generator: one direct input and one through inverter A19. The bearing angle generator consists of a sin/cosine potentiometer and encoder that are motor driven. The encoder outputs drive the Nixie tube front

panel display to show the tracking degrees and supplies the remote track printout signals. The output of the sin/cosine potentiometer is fed to signal/noise summing amplifiers A30 and A31. The outputs of these two amplifiers are then sent to the dual-balanced modulator where the signals are processed as described in DIFAR above. The output of summing amplifier A42 is the input to the four DIFAR output amplifiers A44 through A47.

4.1.6 DEMON Mode:

The DEMON mode simulates amplitude modulation of a LOFAR sonic signal. The 2.5 Hz, 37.5 Hz, and 75 Hz oscillator outputs are fed into amplifier A17 whose output is sent to the DEMON modulator, M3. This modulator amplitude modulates the noise with the three target frequencies. The modulation level is one percent for each target frequency. The M3 output is then passed through filter F1 to attenuate any signal outside the 10-2400 Hz pass band and is fed to the four DIFAR output amplifiers A44 through A47.

4.1.7 ASSG Mode:

The ASSG mode is present to accept a signal from the AN/AQA-7(V), isolate it, and retransmit an identical signal out the four DIFAR and the four OMNI SEARCH amplifiers, A44 through A51.

The input is received in amplifier A43 where the signal level is reduced by a factor of eight. It is then fed to the output amplifiers, whose gain is eight, to provide outputs identical to the input.

4.1.8 BITE Mode:

A BITE mode is present to simulate the BITE circuitry in the AN/AQA-7(V).

The outputs of the BITE DIFAR signals are fed into a signal and noise summation network where the BITE signals are combined with the three uncorrelated noise sources from the multiplexer. These outputs are then sent to a filter and summation network where the 7.5 kHz pilot and 15 kHz carriers are induced to provide an output that is represented by Figure 4-1. This composite is then sent to the four DIFAR and four OMNI SEARCH output amplifiers, A44 through A51.

4.2 PASSIVE MODE DETAILED THEORY OF OPERATION:

The following paragraphs describe the operation of each printed circuit card in the Passive Mode section of the Simulator. It is necessary to refer to the individual schematics while reading each section.

4.2.1 Oscillators* (Reference schematics 14973, 14975, 14986, 14988, 14990, 14992, 14994, 14996, 14998, 15000, 15004, 15006, 15008, 15010, 15012, 15014, and 15017):

Operation of each of the oscillator cards is similar. Some of the cards contain only one oscillator, while others contain two, but each card provides two different output frequencies. The cards with only one oscillator have outputs that are harmonically related.

The frequency source is a crystal controlled oscillator with the crystal frequency between 100 KHz and 200 KHz. The oscillator output is applied to one or more divider circuits to obtain the desired frequency. The square wave output of the divider circuit is passed through an active low pass filter. The resulting output is a sinusoid at a single frequency.

As an example, schematic 15008 utilizes two crystal oscillators to achieve the 1325 Hz and 1700 Hz outputs. IC1, IC2, IC5, and IC6 are the divider circuits and IC3, IC4, IC7, and IC8 are the active low pass filters. Schematic 14998 utilizes only one

*The oscillator cards are nonrepairable subassemblies which must be replaced in the event of an oscillator malfunction. Filter circuits of each oscillator are individually turned to achieve required accuracy and stability.

crystal oscillator to achieve the 800 Hz and 2400 Hz signals since these two outputs are multiples of one another.

4.2.2 Signal Summing (PASSIVE) (Reference schematics 14961, 14963, 14965, and 14967):

The purpose of the signal summing circuits for normal and extended DIFAR NS and EW is to combine ten separate target frequency inputs into a single output. This is accomplished by utilizing linear summing amplifiers. IC2 is included to reduce the loading on IC1. The IC2 output consists of five target frequencies but loads the IC1 amplifier the same as one direct input. Each input is adjustable to control the output level.

Operation of the LOFAR, ALI LOFAR, and DIFAR omni target summing amplifiers is similar to the above circuits. Amplifiers IC1 and IC2 are the summing amplifiers. Their outputs are routed to both IC3 and IC4 summing amplifiers. The configuration shown allows even loading and outputs to DIFAR OMNI, ALI LOFAR, and LOFAR.

The TRACK signal summing board operation is also similar to the above except that the summed signals must also be inverted. The three target frequencies are summed by IC2. The IC2 output provides the necessary positive input to the target bearing generator. It is routed back (external to the schematic) to pins H and T. The input on pin H is passed through inverter IC3 to

provide the negative input to the target bearing generator. The input on pin T is combined with the noise in IC1 which provides the omni Track composite.

4.2.3 Signal and Noise Summing (PASSIVE) (Reference schematics 14948, 14950, and 14952):

Operation of the signal and noise summing circuits is essentially identical in all of the passive mode circuits. The noise and target frequencies are passed through potentiometers to a linear summing amplifier. The potentiometers permit calibration of the signal and noise levels. The relays shown are controlled by the front panel extended/normal band switch (S13) and/or the signal/noise level switch (S4).

4.2.4 7.5 kHz and 15 kHz Signal Generator (Reference schematic 14926):

The 7.5 kHz and 15 kHz signals are used as pilots in the output. 15 kHz signals are also used as carriers in the dual balanced modulator. The purpose of this circuit is to develop these signals and assure that the 7.5 kHz and 15 kHz pilots are frequency locked.

Transistors Q1, Q2, and Q3 and associated parts comprise a crystal controlled oscillator which develops a 120 Hz source

frequency. This signal is fed into driver Q4 whose output is fed into IC2. IC2 is a divide by two circuit which supplies a 60 kHz input to IC3. IC3 is a divide by four circuit which supplies 15 kHz at 0°, 90°, 180°, and 270° to the balanced modulator for use as carriers.

The 15 kHz$\underline{/180^{\circ}}$ from IC3 is also sent to a divide by two circuit through inverter IC1 (yields 15 kHz$\underline{/0^{\circ}}$) to develop the 7.5 kHz pilot. The 7.5 kHz output is sent to amplifier Q6, then to emitter follower Q7. The Q7 output is fed into a band-pass filter and then into the output emitter follower.

The 15 kHz$\underline{/270^{\circ}}$ signal is used to develop the 15 kHz pilot in the composite system output. This signal is inverted, yielding 15 kHz$\underline{/90^{\circ}}$, and fed into amplifier Q5. The Q5 output is fed into a phase adjust circuit. The phase adjust circuit is used to adjust the 15 kHz pilot phase to the phase of the sideband signals developed in the modulator. The output of the passband filter is fed into a Darlington circuit, Q8 and Q9, to provide isolation between the source and load. The phase is a critical parameter; the Darlington circuit prevents loading of the signal source.

4.2.5 Modulator Driver (Reference schematic 14935):

The purpose of the modulator driver is to accept the directional signal inputs and provide that signal and the inverse of that signal to the modulator, each with a given gain. This is

accomplished by using inverting operational amplifiers. The signal is received by one op amp, e.g. IC1, and is inverted. This becomes the $\overline{E}$ output and is also used as the input to the second stage, e.g. IC2. This second stage reinverts the signal and provides the E output. Each has the required drive from the amplifier. The omni portion of the input, E_o, passes through a linear phase filter to compensate for filtering in previous circuits.

4.2.6 Modulator and Summation (Reference schematic 14929): The purpose of the modulator and summation board is two-fold: (1) develop the EW and NS sidebands of the DIFAR composite; and (2) develop the total composite by summing the 7.5 kHz and 15 kHz pilots, the original omni signal and the two sidebands developed in (1).

The 15 kHz pilots from the 15 kHz generator are fed into a complementary amplifier to assure a low impedance drive to the FET for faster switching time. This output drives a FET whose output is modulated by the NS and/or EW signals to develop the necessary sidebands. The modulating signals, the sidebands, and the 15 kHz pilot from the 15 kHz generator are all brought to the same point. The result: the E_{NS} and $\overline{E}_{NS}$ cancel each other and the E_{EW} and $\overline{E}_{EW}$ cancel each other.

This leaves only the EW and NS sidebands and the 15 kHz pilot which are fed into amplifier IC1. The circuit containing A13 and Q14 is a feed-forward network which improves the slew rate of IC1.

The IC1 output is sent to summing amplifier IC3 through the active linear phase lowpass filter, IC2, which attenuates any harmonics. The 7.5 kHz pilot and the original omni signal are also sent to amplifier IC3. The resulting output is a low level DIFAR composite represented by Figure 4-1.

The composite output is also fed into the Q15 and Q16 circuit. This is a bandpass filter, demodulator, and lowpass filter which is used for the 15 kHz pilot phase adjust during calibration.

4.2.7 Relay Passive (Reference schematic 15023):

The relay circuit serves as an interface between the front panel switches and the circuits. Operation of the relays are controlled by the switches such that a given switch setting on the front panel either activates or deactivates a relay to complete the selected circuit. For example, selection of the LOFAR mode on S2 of the front panel will activate relay K3. This closes the normally open contacts, K3A and K3B, completing the circuit between pin Y and pin 9 allowing the LOFAR signal to pass to the GRAM output amplifiers and between pin Y and pin 2 allowing the LOFAR signal to pass to the OMNI SEARCH output amplifiers.

4.2.8 Output Amplifier (Reference schematic 14981):

The output amplifier board consists of two output amplifiers. The passive section requires four boards (8 output amplifiers) and the active section uses one (2 output amplifiers). The relay at the input provides the switching to input either the BITE signal or the mode signal in the passive mode and Range A and Range B outputs in the active mode. The amplifiers are adjustable to provide a nominal gain of eight.

The output amplifiers are complementary Class B to provide balanced drive for both the negative and positive portions of the signals. Transistors Q1 and Q2 provide a low impedance balanced drive to the complementary emitter followers. The complementary setup provides equal output impedance on both the negative and positive cycles. The complementary emitter followers also provide equal impedance for negative and positive portions of the output signals. Resistor, R8, is the balance potentiometer.

4.2.9 Noise Filters (Reference schematics 14863, 14866, 14938, and 14944):

There are seven noise filters in the system: three passive mode 10-2400 Hz; three BITE 10-2400 Hz; and one active mode 350-1350 Hz. The noise source is a pseudorandom

code generator whose output is a $\frac{\text{SIN X}}{\text{X}}$ function. The noise band requirements in the DIFAR System Simulator are such that only small bands of the output of the PRN generator are required.

The number of filtering stages used is determined by the attenuation requirement for the pass band. Each amplifier is driven by an RC network and the combination of the two makes up a filter section. The multiloop feedback incorporated provides stability and gain locking. The total filter is built by cascading low and high pass sections of the proper cutoff frequency.

As an example, reference schematic 14944, which is the EW and NS noise filter for the passive section. These filters are 10-2400 Hz passband. The input stage, Q1, is a clamping circuit which allows the input to the filters to be controlled. The filter is comprised of four stages. The high-pass filter, which achieves 40 db of attenuation between 1 Hz and 10 Hz, is a 3-pole filter consisting of IC1, its input RC network and the RC network on the IC1 output. At the high end, 40 db of attenuation must be accomplished between 2400 Hz and 7500 Hz; slightly more than one octave. To meet this requirement, three stages of 2-pole low pass filtering (6 poles total) are required. These stages are comprised of amplifiers IC2, IC3, and IC4 and their respective input RC networks.

The BITE filters are also 3-pole high-pass and 6-pole-low pass. The active mode filter is 4-pole low-pass and 4-pole high-pass.

4.2.10 DEMON Modulator and OMNI Noise Filter (Reference schematic 14938):

The purpose of the DEMON modulator is to modulate the omni noise with three target frequencies.

The modulating signals are fed through amplifier IC1 to driver Q2. The omni noise is sent through amplifier Q1 to Q3. The output of Q3 is modulated by the Q2 output. This modulated signal is fed to the filter network through emitter follower Q4. The filter network is a 3-pole high-pass and 6-pole low-pass network. IC2 is a 2-pole high-pass active filter, C15, R37, and R38, a 1-pole high-pass passive filter, and IC3, IC4, and IC5, are each 2-pole low-pass active filters. The resultant output is modulated omni noise between 10 and 2400 Hz.

4.2.11 TRACK Bearing Angle Generator:

All particulars of the TRACK bearing angle generator are described in Appendix I.

4.2.12 Remote TRACK and ASSG Input Amplifiers (Reference schematic 15017):

The purpose of these amplifiers is to provide the proper impedance to the signal source and the proper gain to render the inputs usable in the system. The input impedance is established by the resistor network at the input of each amplifier. The gain of each amplifier is adjustable through the feedback potentiometers. The relays on the output of the Remote TRACK amplifiers are controlled by the TRACK bearing LOCAL/REMOTE switch on the front panel.

4.2.13 6° Pulse Decoder (Reference schematic 15020):

When operating in the TRACK mode, the Simulator is required to provide an alert signal everytime the target bearing generator passes through 6 degrees. The purpose of the 6° pulse decoder is to read the BCD output of the target bearing generator encoder and supply an output pulse every six degrees.

The BCD inputs are received by counters IC3 (units), IC2 (tens), and IC1 (hundreds). Each time IC3 counts a 0, 2, 4, 6, or 8 input, IC30 is triggered, directly or through IC31. This provides one input to NAND gate IC4 at the output. The gating is set up such that when IC2 is on a count of 0, 30, 60, or 90 and IC1 is zero, IC4, at the output, is triggered by a count of 6 from IC3.

When IC3 is zero and IC2 is a count of 10, 40, or 70, IC4 is triggered by a count of 2 or 8 on IC3. When IC3 is 20, 50, or 80, IC4 is triggered by a count of 4 by IC3. This continues with IC1 equal to one, two, or three in that an output pulse is provided every 6 counts by IC3.

4.2.14 Remote TRACK Output (Reference schematic 14978):

The Remote TRACK output circuit is incorporated to provide the BCD code from the encoder in the track target bearing generator to a remote printer. The printer is to be triggered by the 6° alarm signal as is the alarm lamp on the front panel.

The 6° pulse signal is received from the 6° Pulse Decoder circuit. This pulse accomplishes two objectives: (1) lluminates the alarm lamp on the front panel through the lamp driver circuits, Q1 and Q2, and supplies the printer trigger command through amplifier A7-5 and NAND gate IC5-2. The BCD code is passed through drivers IC2 and IC7 to NAND gates IC1, IC3, through IC6 and IC8.

4.2.15 DL Mode (Reference schematic 14932):

The DL mode provides a single target frequency of 950 Hz at selectable cardinal or intercardinal bearings and at three signal levels in a noise background. This circuit provides the switching

and signal weighting necessary to simulate the bearing and signal level selected on the front panel and provides the signal/noise summing.

The 950 Hz signal is received on pin Z. Resistors R3, R4, or R5 determine the signal level. With front panel switch S4 in position 3, relays K6 and K7 remain in the position shown, and R3 determines the signal level. With S4 in position 2, K6 selects R4, and with S4 in position 1, K6 and K7 select R5. This signal is sent to amplifier IC1.

Amplifier IC1 output is sent to summing amplifier IC3 where the DL target is combined with the noise. The IC3 output is the omni portion of the DL composite (see Figure 4-1). The IC1 output is also sent to IC2 where it is inverted. Therefore, the IC2 and IC3 outputs are 180° out of phase.

The objective of the circuit is to switch the IC2 and IC3 outputs to IC4 and IC5 to obtain the EW and NS outputs. Table 4-2 provides a matrix which shows which polarities and signal levels are required for each bearing, and the position of relays K1 through K5 required to achieve the output. The OFF relay condition is the condition shown on the schematic.

The purpose of K5 is to switch in resistors such that the input to IC4 and IC5 at intercardinal headings is 0.707 times the inputs

TABLE 4-2

DL MODE SWITCHING

Bearing	SIGNAL LEVEL AND POLARITY		RELAY POSITION REQUIRED				
	NS	EW	K1	K2	K3	K4	K5
0°	+1	0	ON	OFF	OFF	OFF	ON
45°	+ .707	+ .707	ON	ON	OFF	OFF	OFF
90°	0	+1	OFF	ON	OFF	OFF	ON
135°	- .707	+ .707	OFF	ON	ON	OFF	OFF
180°	-1	0	OFF	OFF	ON	OFF	ON
225°	- .707	- .707	OFF	OFF	ON	ON	OFF
270°	0	-1	OFF	OFF	OFF	ON	ON
315°	+ .707	- .707	ON	OFF	OFF	ON	OFF

Note 1: Signal levels are relative.

Note 2: The relay OFF condition is the position shown on the schematics.

at cardinal headings. IC4 and IC5 are signal/noise summing amplifiers. Their outputs are sent to the dual balanced modulator.

4.2.16 BITE Circuits:

The BITE circuits supplied in the DIFAR System Simulator are identical to the BITE circuits in the AN/AQA-7(V). Reference the AN/AQA-7(V) Operation and Maintenance Manual for the detailed theory of operation. The following schematics are included in the BITE circuits.

Title	Schematic Number
Target Summation	14872
Modulator and Filter	14875
Target Generator	14869
Noise Filter	14863
Pseudorandom Code Generator	14860
BITE Oscillator and Active Noise Filter	14866

4.3 ACTIVE MODE SYSTEM THEORY OF OPERATION:

The Active mode of operation simulates received sonar signals. The system output is best described as a pulse train that lasts for 16 seconds. Figure 4-3 is a time bar chart that shows all of the possible outputs within the 16-second operating period.

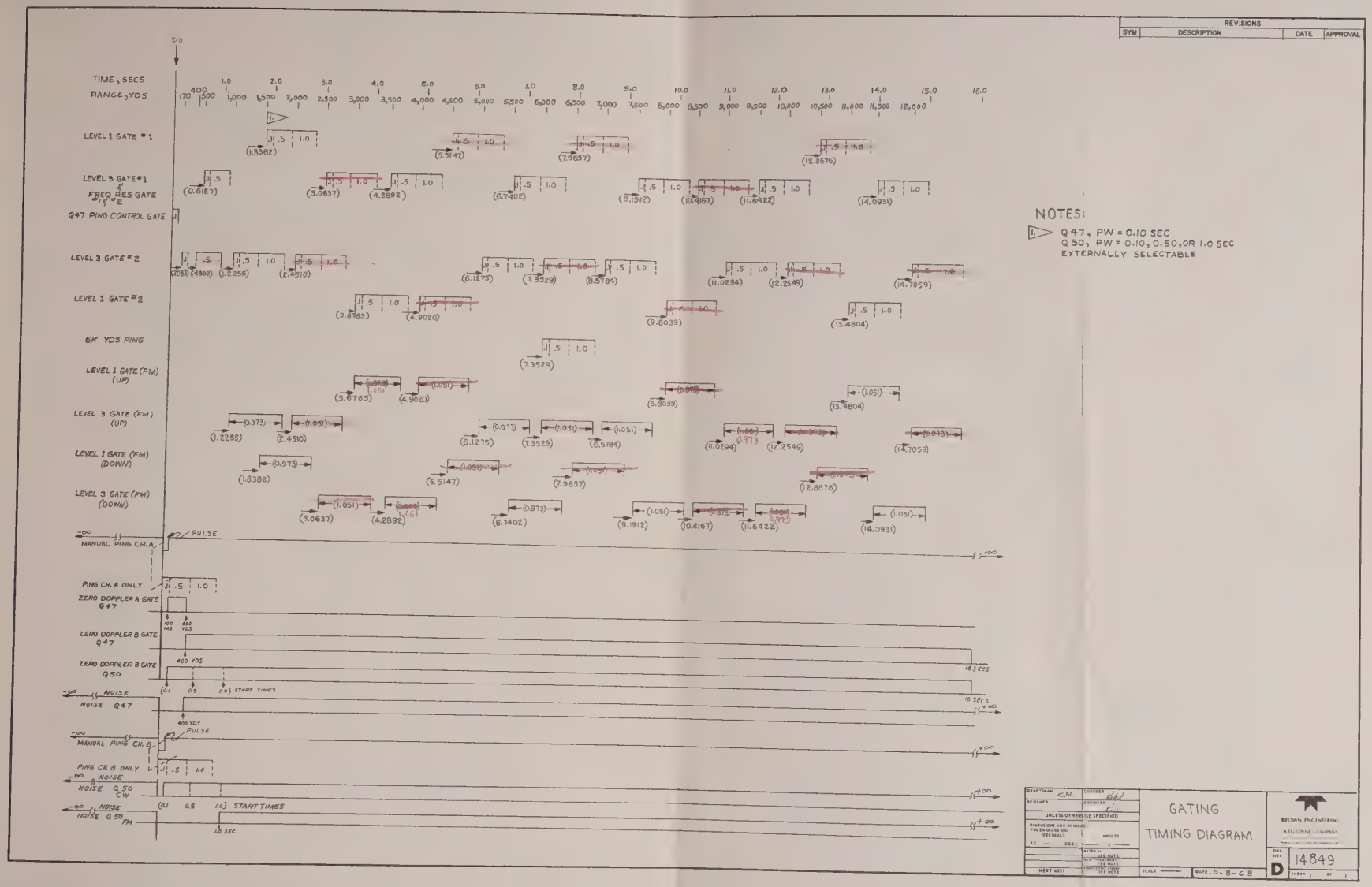
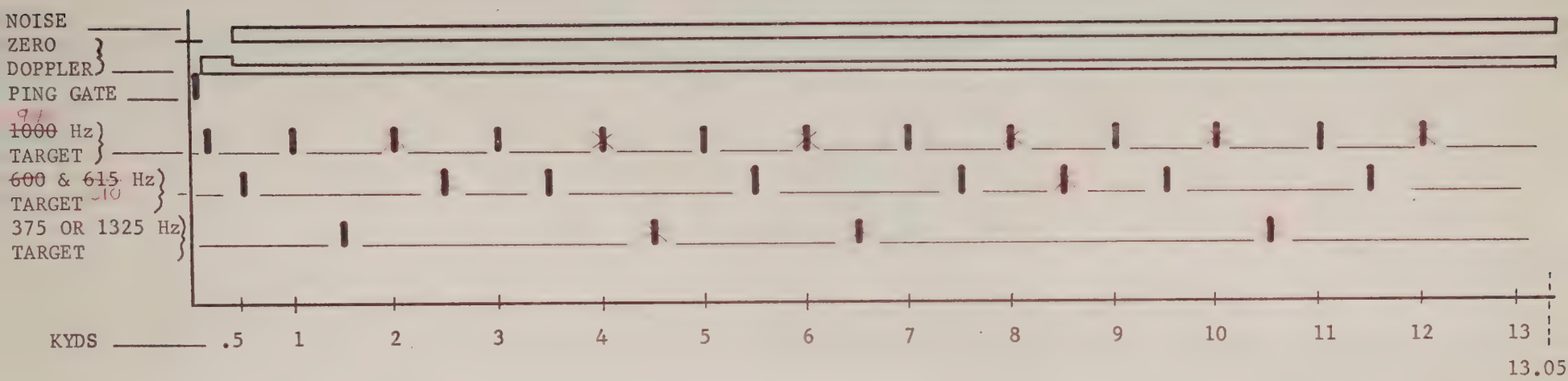


FIGURE 4-3. ACTIVE MODE TIME CHART

The pulses present and length of the pulse in any given cycle is dependent upon the submode of operation and the switch settings on the front panel. The submodes available are Q47, Q50 CW with pulse width of .1, .5, or 1.0 seconds, and Q50 FM. Figures 4-4, 4-5, and 4-6 show the outputs present for each of the active modes. Table 4-3 provides a tabular presentation of the same information and indicates the signal level of each target. The system is required to present a signal-to-noise ratio at one of two levels. This is accomplished by holding the noise constant and varying the signal strength.

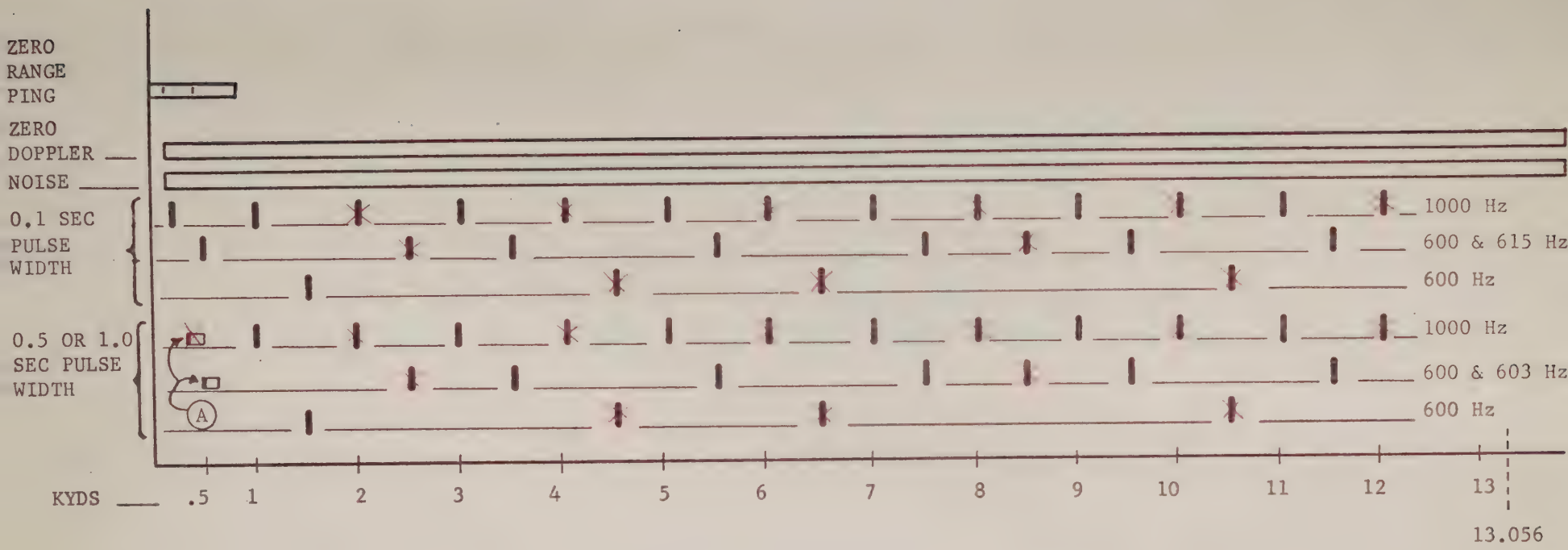
The following paragraphs describe the system operation with the differences between each of the three submodes noted. Refer to Figure 4-7 while reading the system theory.

The Target Time Generator (TTG) utilizes an 816 Hz reference for the time base. Sound travels 816 yards (two way) in one second, therefore, each cycle of the 816 Hz signal represents one yard in target distance. When the TTG receives a start pulse, it issues start commands to the gate control circuitry. As the time progresses, it issues pulses at the required times (yardage) which activates the gate control circuitry. The Target Time Generator Gates group these target pulses such that certain targets activate a given set of circuits in the gate



Ping Gate is a 0.1 second 26 KHz or 38 KHz pulse.
Zero Doppler is a 750 or 950 Hz continuous output starting at T + 0.1 second, with a decrease in amplitude at 400 yards.
Noise is a continuous output starting at T + 0.4902 second (400 yards).
The 1000 Hz, 600 Hz, 615 Hz, 375 Hz and 1325 Hz targets, are 0.1 second pulses. The 375 Hz target corresponds to the 750 Hz zero doppler selection and the 1325 Hz target to the 950 Hz zero doppler.

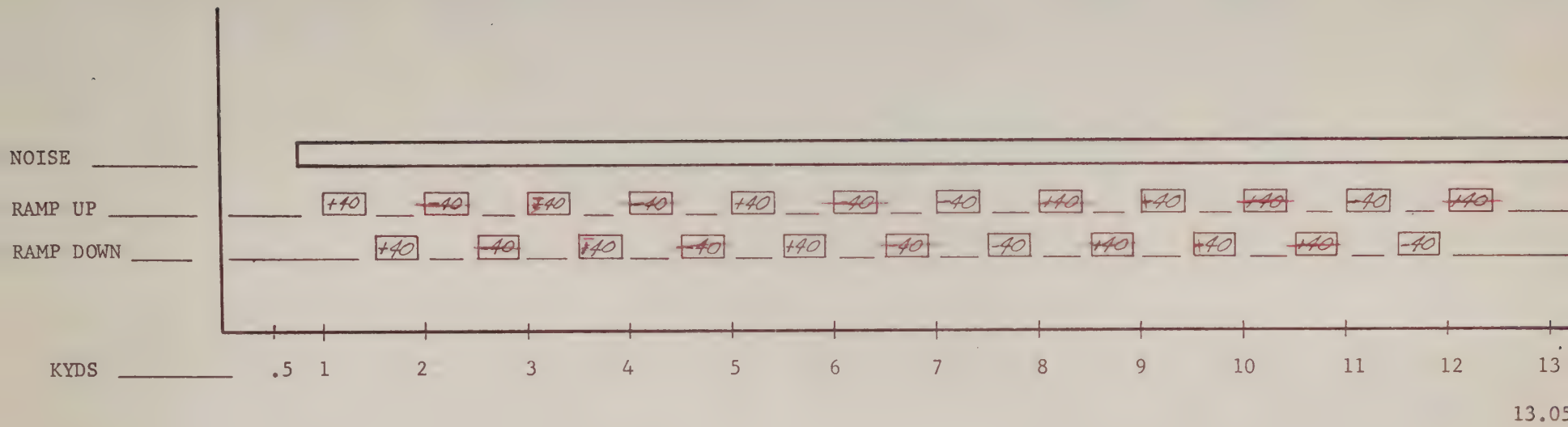
ACTIVE RANGING AUDIO
OUTPUT PULSE TRAIN
Q47
FIGURE 4-4



NOTES: (A) Q50 CW 0.5 SEC PULSE WIDTH ONLY

Zero Range Ping lasts for the ping width selected (.1, .5 or 1.0 second).
Zero Doppler is a 800 Hz continuous output that begins when the zero range ping ends.
Noise is a continuous output that begins when the zero range ping ends.
The 1000 Hz, ~~600 &~~ 615 Hz, ~~600 &~~ 603 Hz are target frequency pings that begin at the time shown an last for the ping width selected.

ACTIVE RANGING AUDIO
OUTPUT PULSE TRAIN
Q5C CW
FIGURE 4-5



Noise begins at t_o + 1 second and continues for the remaining 15 seconds.
For the ramp up or ramp down modes, the +40 and -40 ramps occur at the ranges shown.

ACTIVE RANGING AUDIO
OUTPUT PULSE TRAIN
Q50 FM
FIGURE 4-6

TABLE 4-3

RANGE DATA

Range	MODE TARGET FREQUENCIES (Hz) Q47 .1 Sec.	Q50 .1 Sec.	Q50 .5 Sec.	Q50 1.0 Sec.	SIGNAL LEVEL	Q50 FM RAMP UP	DOWN
170	1,000	1,000	-	-	Level 3	-	-
400	-	-	1,000	-	Level 3	-	-
500	600/615	600/615	600/603	-	Level 3	-	-
1,000	1,000	1,000	1,000	1,000	Level 3	+40	-
1,500	375/1325	600	600	600	Level 1	-	+40
2,000	1,000	1,000	1,000	1,000	Level 3	-40	-
2,500	600/615	600/615	600/603	600/603	Level 3	-	-40
3,000	1,000	1,000	1,000	1,000	Level 1	-40	-
3,500	600/615	600/615	600/603	600/603	Level 3	-	-40
4,000	1,000	1,000	1,000	1,000	Level 1	-40	-
4,500	375/1325	600	600	600	Level 1	-	-40
5,000	1,000	1,000	1,000	1,000	Level 3	+40	-
5,500	600/615	600/615	600/603	600/603	Level 3	-	+40
6,000	1,000	1,000	1,000	1,000	Level 3	-40	-
6,500	375/1325	600	600	600	Level 1	-	-40
7,000	1,000	1,000	1,000	1,000	Level 3	-40	-
7,500	600/615	600/615	600/603	600/603	Level 3	-	-40
8,000	1,000	1,000	1,000	1,000	Level 1	+40	-
8,500	600/615	600/615	600/603	600/603	Level 3	-	+40
9,000	1,000	1,000	1,000	1,000	Level 3	+40	-
9,500	600/615	600/615	600/603	600/603	Level 3	-	+40
10,000	1,000	1,000	1,000	1,000	Level 3	+40	-
10,500	375/1325	600	600	600	Level 1	-	+40
11,000	1,000	1,000	1,000	1,000	Level 1	-40	-
11,500	600/615	600/615	600/603	600/603	Level 3	-	-40
12,000	1,000	1,000	1,000	1,000	Level 3	+40	-

Note 1: Yardage is measured to leading edge of returns (from leading edge of ping).

Note 2: Nominal velocity in water is 816 Yard/Second (2 way).

Q47

E9 - CL-F 1325 HZ or 375 HZ
1.5 Kyds

E3- CLN 990 HZ
170 yds 1Kyds 5Kyds 7Kyds 9Kyds

E10 - CLK 990 HZ
3Kyds 11Kyds

E2 - CL-C 610 HZ
500 yds 3.5Kyds 5.5Kyds 7.5Kyds 9.5Kyds 11.5Kyds

Q50-.1

E3 CLN 990 HZ
170 yds 1Kyds 5Kyds 7Kyds 9Kyds
E10-CLK 990 HZ

3Kyds 11Kyds
E2 CL-C 610 HZ
500 yds 3.5Kyds 5.5Kyds 7.5Kyds 9.5Kyds 11.5Kyds
E9-CLF 610 HZ
1.5Kyds

Q50-.5

E6-B1U 994 HZ
1Kyds 5Kyds 7Kyds 9Kyds

E14 B1X 994 HZ
3Kyds 11Kyds

E8-CL-A 606 HZ
500 yds 3.5Kyds 5.5Kyds 7.5Kyds 9.5Kyds 11.5Kyds
E1-CL-C 606 HZ
1.5Kyds

Q50-1.0

E6-B1-U 994 HZ
1.0Kyds 5.0Kyds 7.0Kyds 9.0Kyds
E14-B1-X 994 HZ
3.0Kyds 11.0Kyds
E8-CL-A 606 HZ
3.5Kyds 5.5Kyds 7.5Kyds 9.5Kyds 11.5Kyds
E1-CL-C 606 HZ
1.5Kyds

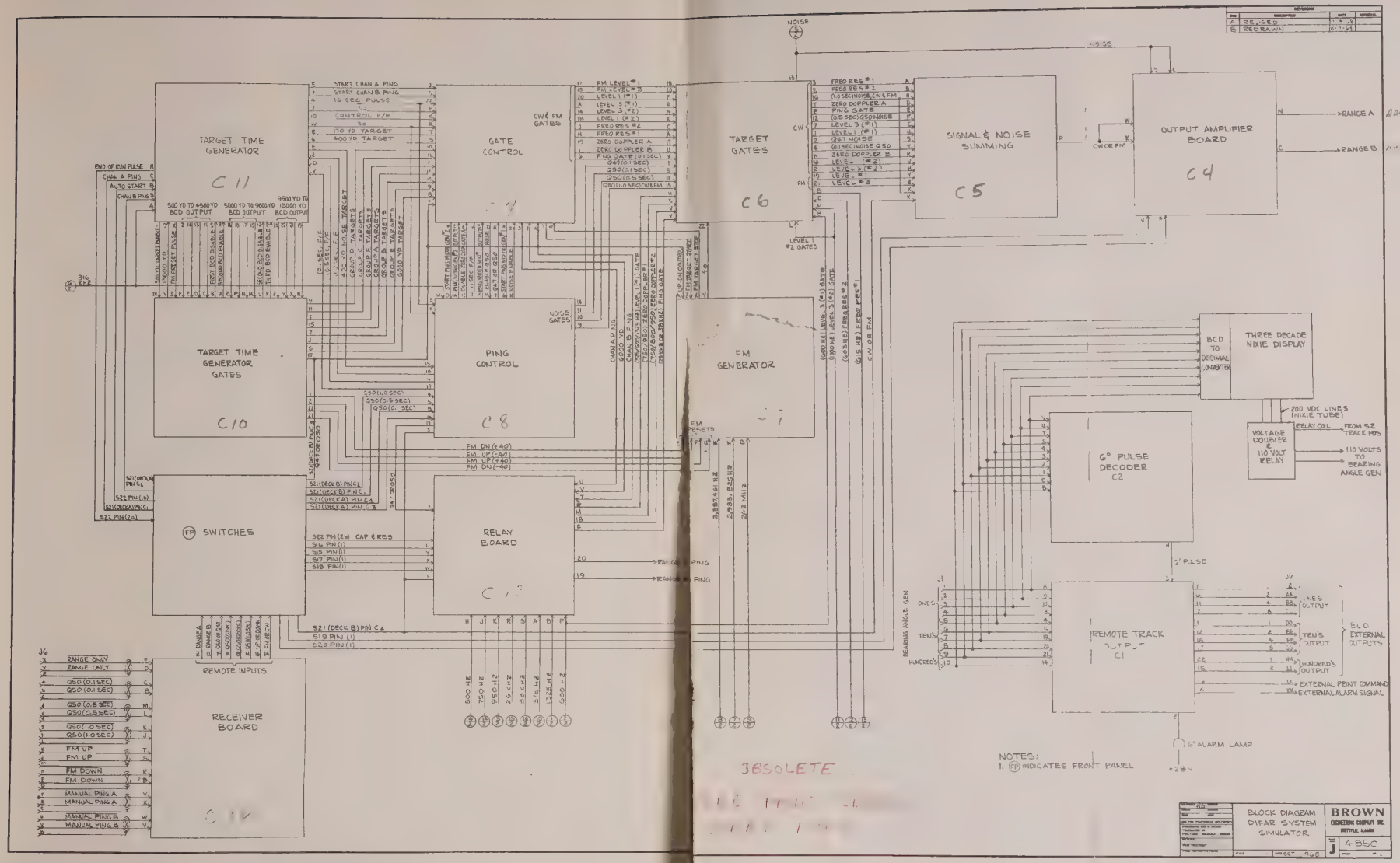


FIGURE 4-7. ACTIVE MODE FUNCTIONAL BLOCK DIAGRAM

control circuitry. When the TTG counts to 16 seconds (13, 056 yards), it issues an end-of-run pulse to the automatic/manual switch, S22. If in manual mode, operation ceases. If S22 is in the AUTO position, the end-of-run pulse serves as the start pulse to the TTG and the cycle begins again. If the system is set to Q50 FM, the FM Generator accepts preset signals from the Target Time Generator. These presets occur 10 yards prior to target time. Their purpose is explained in the description of the FM Generator.

The Ping and Gate Control circuits receive the timing pulses from the Target Time Generator. These inputs accomplish two things: (1) activate a ping width generator which produces the required ping width; and (2) activate the circuits which control the target gates. When a pulse is received, the ping width generator starts and the gate control circuits open a gate, or set of gates, in the Target Gate circuits. When the ping width time has elapsed, the ping width generator deactivates the gate control circuits which then deactivates the Target Gates it had selected. The pulse width is 0.1 second for Q47. Q50 CW pulse widths are either 0.1, 0.5, or 1.0 seconds as selected by S25 on the front panel or the remote control. The ping widths in Q50 FM are controlled by the FM Generator.

The Target Gate Circuits are gates which serve as an interface between the oscillators and the audio output amplifiers. When commanded by the gate control circuits, the selected gate, or gates, allow a signal to pass. When the command is removed, the target gates provide a ground. The sinusoid signal source is the oscillators discussed in passive mode of operation for the CW signals. In addition to the target frequencies, the target gates also pass noise. The noise and target frequencies are combined in an output summing amplifier whose output becomes the Range A and Range B audio outputs.

When the system is operating in Q50 FM mode, the audio outputs are square wave ramps instead of sinusoids. These ramps are generated by the FM Generator. The concept is to frequency modulate a reference signal, and filter the output to provide the desired ramp. The requirement is to generate a ramp with the option to ramp UP or DOWN between two frequency bands. These ramps represent the return from ramp UP or DOWN ping. The lower band represents targets going and the upper band represents targets coming.

This FM Generator produces the ramps with digital circuits. The principle for the FM generator is to take a high frequency signal and frequency modulate this signal to produce a frequency

with ramping characteristics. The signal to be modulated is a 2.42 MHz oscillator and the modulating signal is either 3,387.5 or 2,983.8 Hz. The frequency modulation is accomplished by feeding the 2.42 MHz into one counter, one of the modulating signals into another counter, and comparing their outputs which are fed to a flip-flop. The on time for the flip-flop will be in proportion to the desired frequency. For a ramp up, the comparator circuit triggers a NAND gate each time the counter binary outputs are equal. For a ramp down, the comparator triggers the NAND gate when the binary equivalent of one counter is the complement of the binary equivalent of the other counter.

For each count of the modulating signal counter, the 2.42 MHz counter will count and reset several times. As the modulating counter progresses for a FM up ramp, the output FF allows the 2.42 MHz frequency to pass longer in each time period. This provides an output represented by Figure 4-8.

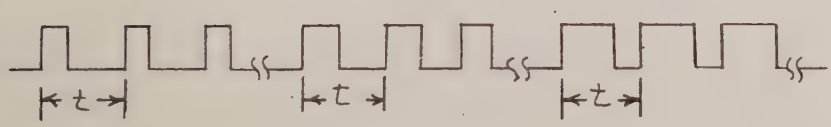


Figure 4-8. FM Ramp

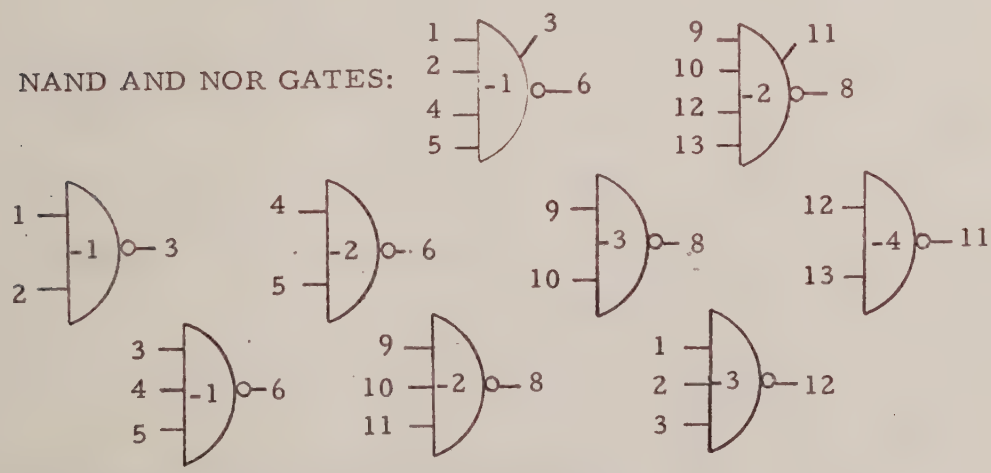
When this signal is passed through a divide by 2000 circuit, the output is an FM ramp that changes in steps.

The modulating signal is also fed into a counter that is preset to complete its count in the same time it takes to generate a ramp. When this counter reaches the required time, its output clears the ramp counters and triggers the gate control circuitry which deactivates the target gates.

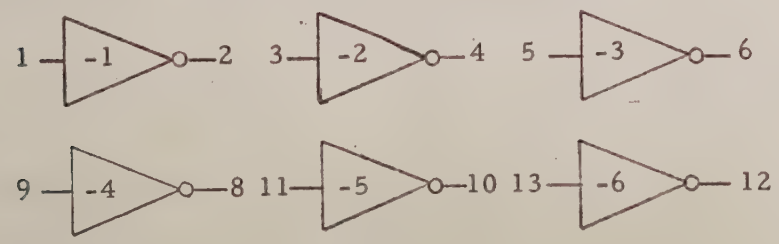
4.4 ACTIVE SECTION DETAILED THEORY OF OPERATION:

The following paragraphs describe the operation of each printed circuit card in the Active Mode section of the Simulator. The following key identifies the dash number for integrated circuit reference designations:

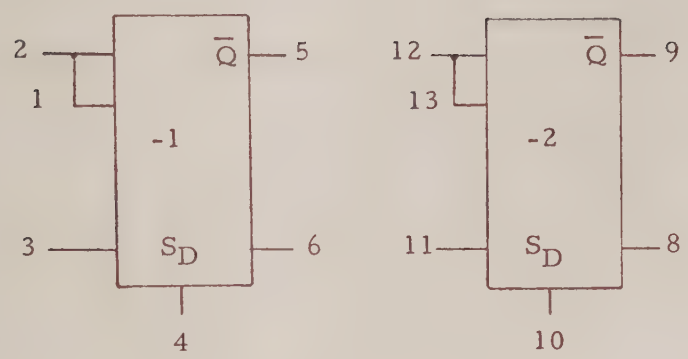
NAND AND NOR GATES:



DRIVERS, BUFFERS AND INVERTERS:



FLIP-FLOPS:



4.4.1 Target Time Generator (Reference schematic 14885):

The Target Time Generator provides output pulses at the required time and establishes the 16-second operating cycle. The time base is a 8.16 kHz signal which is divided by 10 by IC1. The resulting 816 Hz signal provides one cycle in the time it takes sound to travel one yard (2 way) in water.

Operation is initiated by a command through pin B, C, or 3. IC19-4 is a NOR gate which sets IC25-2. The output of IC25-2 serves as one of the inputs to NAND gate IC19-3. The second input to IC19-3 is the 816 Hz reference which triggers IC19-3 to insure a start time in phase with the 816 Hz signal. The IC21-3 output is fed back to IC25-2 as a reset pulse. The IC21-3 output also sets IC25-1 which triggers NOR gate IC12-4 and provides the start channel A ping command to the gate control circuits.

The NOR gate IC12-4 output is inverted by IC21-2 whose output drives IC21-6 to provide the 16-second pulse command to the ping control board and to IC21-1 which provides an input to NAND gate IC2-1. The IC21-2 output also triggers one shot IC4-1. IC4-1 provides the t_o and $\overline{t_o}$ commands to the ping and gate control boards, and clears the Target Time Generator counters.

The start signal (pin B, C, or 3) also triggers IC19-1 NOR gate which sets F/F IC9-2. The IC9-2 output provides the third of 3 required inputs to NAND gate IC2-1. IC2-1 is therefore enabled from t_o to 13,000 yards.

The output of IC2-1 is the input for a divide by five circuit which is made up of IC9-1, IC8, IC2-3, and IC3-2. Each cycle of the input to the divide by five counter represents one yard; each cycle of the output drives IC6 and IC7, both of which are divide by 10 circuits. Each count to the input of IC6 represents 5 yards. Each count to the input of IC7 represents 50 yards. As IC6 and IC7 reach a desired target, a command pulse is released. When IC6 and IC7 count 34 (5 x 34 = 170 yards), NAND gate IC11-1 is activated, providing the 170 yard pulse to the ping and gate control boards. The 0.1 second FF input, pin Y, comes from the ping width generator to enable the 170 yard target for the 0.1 second

mode of operation. When IC6 and IC7 reach the count of 8 (8 x 50 = 400), the 400 yard target command occurs at the output of IC12-2. IC12-2 output provides the 400 yard noise target to the gate control circuitry, but is only meaningful in the Q47 mode. The 0.5 second FF input, pin D, enables the 400 yard target only for 0.5 second mode of operation. IC16, IC17, and IC18 provide the target pulses to the time generator gates for all target times beyond 500 yards. The first 500 yard target command, output of IC7, pin 6, sets IC20-1 which disables the control F/F. This prevents the 170 yard and 400 yard outputs from occurring in successive counts of IC6 and IC7 (e.g. 670 yards, 900 yards, 1170 yards, 1400 yards, etc.). IC11-2 issues a FM preset signal to the Target Time Generator Gates during every run, but is only meaningful for Q50 FM mode. IC11-2 is gated such that it is triggered by IC6 and IC7 10 yards prior to the target distance.

When IC18 reaches a count of 13,000 yards, this signal is routed to the gate control circuits and back to pin 9. This input triggers IC9-2 to remove the output to NAND gate IC2-1 stopping the yardage counters. It also triggers IC20-2 providing the second input to NAND gate IC19-2; the first input is the 816 Hz reference. This starts a divide by 56 circuit: IC22 and IC23-1 and -2. When this circuit reaches its maximum count, this represents a total count

of 13,056 yards which is equal to 16 seconds. The output of IC23-2 triggers one shot IC24. The output at pin 1 of IC24 resets IC20-2 stopping the divide by 56 circuits, sets IC25-1 cutting off NAND gate IC12-4, and consequently, all downstream circuits, and sends the end of run pulse out pin 8. If the system is in automatic mode, the end-of-run pulse is routed back to the pin B input causing the cycle to start again. If in manual mode, operation of the Target Time Generator ceases.

The previous example was for a manual ping channel A. The channel B ping is the same except the start pulse goes into an identical circuit to produce a start Channel B ping.

4.4.2 Target Time Generator Gates (Reference schematic 14891): The target time generator gates serve to group the target yardage start commands from the time generator. Each group activates a given gate control circuit which opens the proper target gates.

The BCD target inputs to IC3, IC4, and IC5 are received from the target time generator. IC3 decodes the 500 through 4500 yard targets, IC4 the 5000 through 9000, and IC5 the 9000 through 13,000 yard targets. The decoder outputs are routed to NOR gates IC11 through IC14 in groups. These groups are based on the gating requirements indicated in the time bar chart

shown in Figure 4-3. Each group activates different circuits in the gate control circuits.

When operating in Q50 FM mode, the FM preset signal on pin 3 provides a meaningful second command to the FM preset gating. Preset commands are required from 990 yards to 11,990 yards in increments of 500 yards. The first input to IC8-1 NAND gate is present from 500 yards to 999 yards. The FM preset is received at 990 yards which triggers IC8-1 causing the proper preset output. Operation of ping width generator 2 is identical to ping width generator 1.

4.4.3 Ping Control (Reference schematic 14894):

The ping control circuits provide pulse width timing. The timing requirements are 0.1 second for Q47 and 0.1, 0.5, or 1.0 second for Q50 CW. In addition, the ping width generators generate several reset pulses for other functions on the ping and gate control boards.

Prior to a ping command, which may be initiated either locally or from a remote location, the mode conditions must be selected. (For local, all active front panel switches must be in the required position). At time t_o, a pulse strobes the required pulse width into flip-flops IC10-1, IC10-2, and IC20-1. The required pulse width is stored until the end-of-run, or 16 seconds after t_o, at which time the 16-second pulse resets the ping width flip-flop.

Figures 4-3, 4-4, and 4-5 show the required timing outputs. In Q47 mode, the first timing required is deactivate ping control gate after 0.1 second and simultaneously enable Zero Doppler A. This is accomplished in the gate control circuitry through use of ping width generator #1 signal. The next command required is disabling the Zero Doppler A, and enabling Q47 noise and Zero Doppler B. Receipt of the 400 yard noise target command on pin 15 provides the second input to NAND gate IC11-2. This output passes through IC28-6 to the gate control circuits to disable Zero Doppler Gate A. The IC11-2 output also triggers NOR gate IC11-3 which sends a noise enable command through pin N to the gate control circuits and sets IC20-2. With IC20-2 set, IC3-3 is activated to open the Q47 noise gate. When IC20-2 was reset, IC27-1, -2, and -3 also received enabling on one of 3 input gates. If Q50 had been selected, the IC27 corresponding to the mode selected would have the second of 3 required inputs from IC1. Therefore, on receipt of the Q50 noise enable command (pin H), the third required input would be present, providing the noise gate command out pin 9, 10, or 11 to the gate control circuitry.

The outputs from the ping width flip-flop go to the Target Time Generator and to ping width generator 1. The ping width will

be determined according to which gate is enabled. For 0.1 second, gate 15-1 is enabled; 0.5 second gate 17-2 is enabled; and for 1.0 second gate, 17-3 is enabled.

Receipt of the start ping width generator 1 signal on pin 16 provides an input to IC4-1 whose output is one of the required inputs for NAND gate IC5-4. The 8.16 kHz time reference is the other required input for IC5-4. IC5-4 output is the timing input to IC6, IC7, and IC14 which serve as counters; they count the pulses of the 8.16 kHz reference. One of three gates, IC16-1, IC17-2, or IC17-3 has to be enabled by the pulse width flip-flops. When the required number is reached in IC6, IC7, and IC14, corresponding to .1, .5, or 1.0 second, the common output of the three gates goes low. This output pulse goes off the board via pin 19, and is also used to preset the counters to 32. The number 32 is preset into the counter to reduce the required number of decoding gates. The 0.1 second timing is created by decoding a count of 848; 0.5 second timing by decoding 4112; and 1.0 second timing by decoding 8192.

4.4.4 Gate Control (Reference schematic 14888):

The gate control circuits receive timing signals from the target time generator, target time generator gates, and the ping control circuits. These inputs are utilized to energize and de-energize the target gates. Figure 4-3, the time bar chart,

provides the sequencing required. The following description is based on mode Q47 with the differences due to Q50 described as necessary.

The first signals received are t_o, $\overline{t_o}$, 16 second pulse, Q47 or Q50, and Start Chan A or Start Chan B pings. The Q47 command, pin R, provides inputs to NAND gates IC2-1, IC5-4, and IC8-3. The t_o command (pin X) triggers IC5-4 which causes IC3-2 to send the ping gate command to the target gates. This causes the initial 0.1 second ping shown in Figure 4-4. The Start Chan A and Start Chan B inputs cause outputs directly on Range A or Range B gate outputs. These outputs are routed to the relay board where they are controlled by S17 to achieve Range A and/or Range B outputs.

The $\overline{t_o}$ input (pin P), simultaneous with t_o, triggers NOR gate IC2-2 which provides the first start ping width generator #1 command to the ping control circuits. The 16 second pulse, pin 22, directly sets IC3-1. This causes a low condition at pin 1 and prevents Zero Doppler Gate B from passing the reverberation shaping signal.

At the end of 0.1 second, the ping width generator #1 output (pin B) goes low. This provides one necessary low input to IC8-3 for Q47 mode, whose output sets IC3-2. This deactivates

the ping gate, thereby ending the ping after 0.1 second. Also at T +0.1 second, the ping width generator #1 output provides the third input to IC2-1. This triggers IC2-1 whose output sets IC6-2 causing the Zero Doppler Gate A command to begin. This command remains present until the 400 yard target is reached.

At T +.2083 second, the 170 yard target command is received on pin T. This triggers NOR gate IC14-4 whose output passes through NOR gate IC14-1, and IC10-1 to start ping width generator #2 in the ping control circuits, and sets IC13-2. This causes a high at pin 14, energizing level 3 (#2) gate. After 0.1 second has elapsed, the ping width generator 2 command is received in pin E which resets IC13-2 causing the level 3 (#2) gate target gate to open.

When the 400 yard target time is reached, it is necessary to deactivate Zero Doppler A and activate the Zero Doppler B and Q47 noise gate. The noise enable command is received on pin 21. This triggers IC3-1 to enable Zero Doppler Gate B. A disable Zero Doppler Gate A command is received through pin Z which causes the IC6-1 output to go low deactivating the Zero Doppler Gate A target gate. The disenable Zero Doppler Gate B command comes from the 16-second pulse.

The next signal received is the 500 yard target. The command enters the Group D targets, pin 10, and activates IC8-4 which

sets IC9-1. The IC9-1 output opens the level 3 (#2) target gate and starts ping width generator #1 in the ping control circuits. When the ping width time has elapsed, IC9-1 is reset by an input from pin B through IC7-6 and IC7-2. This removes the level 3 (#1) target command. The remaining Group D targets activate the same circuitry.

The 1000 yard target command enters through the Group A targets (pin 12). It activates NOR gate IC14-1 to open level 3 (#2) target gate through IC13-2 and to start ping width generator #2 in the ping control circuits. In Q47 mode, the remaining circuit operation is identical to the 170 yard command above. In the Q50 FM mode of operation, the Group A target command will also trigger NAND gate IC14-2. The second input to IC14-2 comes from the UP and DOWN input on pin F (selected when Q50 FM was selected). IC14-2 output triggers NOR gate IC5-1 which causes IC15-2 to open the FM level 3 in the target gates. The IC5-4 output also triggers IC5-3 NOR gate to start the target timing in the FM generator. In Q50 FM, target timing is dependent on the period of the FM ramp. When the ramp is completed, an input on pin 16 removes the output of IC15-2 causing the FM level 3 to be deactivated. The remaining Group A targets cause the same operation.

The Group A and Group D gate control circuit operation is described above. The remaining target groups cause similar operation in that the target input command activates an output FF that controls the target gate and simultaneously activates either the CW or FM timing circuits. When the pulse width time elapses, the gate control circuits receive an input which deactivates the output FF causing the target gate to de-energize.

4.4.5 FM Generator (Reference schematic 14853):

The purpose of the FM Generator is to present to the target gate circuitry an FM ramp which ramps up (-40) or (+40) or ramps down (+40) or (-40). The ramp desired, up or down, is selected on the front panel. The system concept is to frequency modulate a 2.42 mHz carrier with a 3,387.5 Hz (+40) or a 2,983.8 Hz (-40) signal such that when the modulated output is filtered, the result is an FM ramp between the desired frequencies. The requirement of the two ramps also establishes the length of time the output is desired. This objective is accomplished through digital logic.

This discussion is based on selections of FM UP (S27). This is the requirement for the 1000 yard target. The FM UP command is received on pin A, which provides one of the required inputs to NAND gate IC27-4. The FM UP DOWN level also sets a comparator circuit to compare binary

numbers for up ramp and compare the binary number and its complement for the down ramp. The +40 input (pin F) provides the second input to IC27-4, which then triggers NOR gate IC29-1. The IC29-1 output accomplishes two objectives: the first is to preset a clock (IC7 and IC8) such that it reaches its maximum count in the time it takes to generate the ramp; the second is to trigger IC14-2. An output on pin 9 of IC14-2 serves as one of two required inputs to NAND gate IC27-2. The second input to IC27-2 is the modulating frequency (3.387.5 Hz) from pin M. This oscillator signal is fed to a divide by 16 circuit, IC10-1, and through IC30-3. IC30-3 is a NAND gate which requires a second input. This signal is provided by a FM target start command through pin Z from the gate control circuitry. This command triggers IC15-1, providing a high condition at pin 5, and thereby enabling the IC10-1 clamp to exist, and a low to IC30-2 whose output is the second input to NAND gate IC30-3. This creates two inputs to NAND gate IC27-2 providing the input to the IC7 and IC8 ramp length clock and to the IC4, IC5, and IC6 counter. The IC4, IC5, and IC6 counter output is the modulating signal. This clock output is tied to a comparator circuit that consists of IC20 through IC24, IC25-2, and IC31. The IC4, IC5, and IC6 counter was preset by the +40 input on pin F through IC27-4, IC28-1, IC26-2, and

IC28-4. This preset serves to set the counter for the proper starting frequency.

The 2.42 MHz reference signal is received through pin B and fed into a divide by 605 circuit. This circuit is basicly a counter that provides one output pulse for every 605 input pulses and resets itself after counting through 605. As the divide by 605 circuit is counting, it provides the counts to the comparator circuit as does the IC4-IC6 counter. Each time the count of the IC4-IC6 counter is the same as the IC1-IC3 counter, the comparator circuit triggers NAND gate IC25-2 (IC31-1 and IC31-2 are expanders for IC25-2). When the output of IC25 goes low, this sets IC15-2 whose output goes low, preventing the 2.42 MHz from passing through IC26-1. The divide by 605 counter passes 605 counts faster than the IC4-IC6 counter passes its required count. Therefore, there is more than one output from NAND gate IC25 for each count of the IC4-IC6 counter. Each time IC1-IC3 reaches a count of 605, an output from pin 11 of IC3 triggers IC15-2, which provides the third input to NAND gate IC26 and allows the 2.42 MHz to pass. The output of IC26-1 is represented by Figure 4-8.

As the IC4-IC6 clock count increases, the period at pin 9 on IC15-2 remains constant, and the duty cycle changes. This signal is fed into a divide by 2000 circuit which acts as a filter. The output

becomes a ramp that changes in steps.

The two clocks monitored by the comparator continue to count their respective inputs until the period time clock IC7 and IC8 reaches the required count. The IC8 output (pin 6) triggers IC16 causing IC16, pin 1, to go low and IC16, pin 6, to go high. A target stop pulse is initiated from pin X at the end of a sweep. This same pulse is used to reset the FM generator counters.

4.4.6 Target Gates (Reference schematic 14897):

The purpose of each gate is to pass a given signal when commanded, and provide a ground at the output at all other times. Each of the target gates are identical in operation. This discussion refers to the Q47 noise gate components.

The noise input to Q3 source is present at all times. On receipt of a command from the gate control circuits to the base of Q1, Q1 is turned on and then turns Q2 on. This brings the Q2 collector voltage to a high level, turning on Q3, allowing the noise to pass. When the input to Q1 base is removed, Q1 and Q2 are turned off causing the collector of Q2 to go low (approximately -15V). This turns Q4 on and presents a ground at the output.

4.4.7 Signal and Noise Summing (Active) (Reference schematic 14984):

The function of the signal and noise summing circuit is to combine multiple inputs from the target gates into a single signal for the output amplifier.

Each input enters through a potentiometer to allow individual adjustment. The CW inputs are combined by summing amplifiers IC1 and IC2. IC3 is a summing amplifier which combines the outputs of IC1 and IC2. IC4 is the summing amplifier for the FM ramps and noise in the Q50 FM mode.

This board also provides the relay driver circuit, Q1 and associated parts, for the CW or FM relay. This relay is controlled by the CW/FM switch, S26, on the recessed panel.

4.4.8 Relay (Active) (Reference schematic 14970):

The relay circuit serves to gate the proper input to the target gate circuits. The relays are controlled by the front panel switches. One side of the relay coils are continuously tied to the +28VDC supply. The other side is connected to a front panel switch which provides a ground or open as necessary. For example, if switch S15 on the front panel is set to 26 KHz, relay K4 is in the de-energized position allowing the 26 KHz

oscillator output to pass through the normally closed contact of K4. When 38 KHz is selected, the K4 coil is energized and 38 KHz is supplied through the normally open contact.

4.4.9 Line Receiver (Reference schematic 15037):

The Line Receiver circuits are used as an interface between the Simulator and the signal source when the Simulator is being controlled from a remote station. Each signal received is passed through a buffer prior to being routed to the specific circuit.

4.4.10 Oscillator (Active) (Reference schematics 14973, 14975, and 15014):

Refer to the passive section oscillator theory.

4.4.11 Output Amplifier (Active) (Reference schematic 14981):

Refer to the passive section output amplifier theory.

5.0 CALIBRATION:

For convenience, the calibration procedure for the CD-3800 DIFAR System Simulator is contained in Appendix II.

6.0 MAINTENANCE:

6.1 TROUBLESHOOTING:

This section provides the system user a guide to isolate failures to a line replaceable unit. Not all possible failure effects are covered in detail, but coverage of general modes of failure is sufficient to locate the majority of failures of the system. The Brown Engineering Resident Engineer will provide support for all troubleshooting.

6.1.1 Troubleshooting Guides:

Troubleshooting guides are provided as tables. These tables are broken into functional problems in each mode as listed below:

PASSIVE MODE:

Table 6-1: Noise Problems (Passive)

Table 6-2: Pilot Problems (Passive)

Table 6-3: Target Problems (Passive)

Table 6-4: BITE Problems

Table 6-5: Composite and Miscellaneous Problems (Passive)

ACTIVE MODE:

Table 6-6: Noise Problems (Active)

Table 6-7: Target Problems (Active)

Table 6-8: Timing Problems (Active)

ACTIVE MODE: (continued)

Table 6-9: Total Output and Miscellaneous Problems (Passive)

Each of the guides shows a problem condition followed by the possible causes of the condition. When trying to determine what condition listed fits the condition being experienced, Figures 4-1, 4-4, 4-5, and 4-6 may be of assistance. These figures show what the output consists of in each of the operating modes.

The sequence of possible causes within each condition are in descending order of probability when the difference in probability of occurrence is significant. When more than one cause exists, they should be eliminated in order given. For example, in Table 6-3, the first condition is "all targets missing in all modes". "Switch S31 in OFF position" is shown as most probable cause. Prior to checking the power supplies listed in cause #2, the first step should be to check the S31 position.

Normal operation of the Simulator Active Mode occurs with the Simulator under remote control by the AN/AQA-7(V). When a problem occurs, the first step in troubleshooting should be to set up the same mode, under LOCAL control, in which the discrepancy was noticed. If the problem disappears, this isolates it to the remote source or the Line Receiver, card C12.

Substitution of another Line Receiver will quickly determine where the trouble exists.

The troubleshooting guides are based on the assumption that the Simulator will not operate correctly when under LOCAL control, except for a few cases of improper switch settings which are covered for both LOCAL and REMOTE.

6.2 ROUTINE MAINTENANCE:

Wash the air filter at thirty-day intervals with a mild detergent to remove all dust and grim. Dry the filter by use of compressed air prior to replacing it in the system.

Refer to Appendix I for specific instructions on the Target Bearing Generator Module.

6.3 PREVENTATIVE MAINTENANCE:

To assist in preventing support shutdown or erroneous operation, it is recommended that an acceptance test be performed on the Simulator at six-month intervals. This test verifies many parameters not affected by calibration, and will detect faults that may not be readily noticeable during normal operation.

Acceptance Test Procedure, TP 14900, Volume I, provides a step-by-step method of verifying Simulator performance.

TABLE 6-1

NOISE PROBLEMS (PASSIVE)

CONDITION	POSSIBLE CAUSE	ACTION REQUIRED
Noise not present in any mode	1. S32 is set to OFF 2. PRN generator	1. Set S32 to ON 2. Replace card B15
Omni noise not present or wrong level in all modes	1. S37 is set to OFF 2. Omni noise filter	1. Set S37 to ON 2. Calibrate or replace card B13
Omni noise not present in one mode only	1. Signal/noise summing amplifier	1. Calibrate or replace: a. Card B10 for LOFAR or ALI LOFAR b. Card B12 for DIFAR c. Card A9 for TRACK d. Card A2 for DL e. Card B18 for BITE
NS sideband noise not present or wrong level in all modes, but targets are present	1. NS noise filter	1. Calibrate or replace card B14
NS sideband noise not present or wrong level in one mode only, but targets are present	1. Signal/noise summing amplifier	1. Calibrate or replace: a. Card B12 for DIFAR b. Card B11 for TRACK c. Card A2 for DL d. Card B18 for BITE
EW sideband noise not present or wrong level in all modes but targets are present	1. EW noise filter	1. Calibrate or replace card B14
EW sideband noise not present or wrong level in one mode only, but targets are present	1. Signal/noise summing amplifier	1. Calibrate or replace: a. Card B11 for DIFAR b. Card B11 for TRACK c. Card A2 for DL d. Card B18 for BITE

TABLE 6-2

PILOT PROBLEMS (PASSIVE)

CONDITION	POSSIBLE CAUSE	ACTION REQUIRED
7.5 KHz pilot missing or wrong level	1. S36 set to OFF 2. Summing amplifier 3. Signal generator	1. Set S36 to ON 2. Calibrate or replace card B7 3. Calibrate or replace card B8
15 KHz pilot missing or wrong level	1. S35 set to OFF 2. Modulator or summing amplifier 3. Signal generator	1. Set S35 to ON 2. Calibrate or replace card B7 3. Calibrate or replace card B8
15 KHz pilot out of phase	1. Phase adjust circuit	1. Calibrate or replace card B8
7.5 and 15 KHz pilots missing	1. S35 and S36 to OFF 2. Signal generator	1. Set S35 and S36 to ON 2. Replace card B8
7.5 and 15 KHz pilots are off frequency	1. Signal generator	1. Calibrate or replace card B8

TABLE 6-3

TARGET PROBLEMS (PASSIVE)

CONDITION	POSSIBLE CAUSE	ACTION REQUIRED
All targets missing in all modes	1. S31 is set to OFF 2. Oscillators not ON	1. Set S31 to ON 2. Check power supplies PS3 and PS6 for output
All targets in one mode missing or wrong level	1. S4 set to wrong position 2. S14 set to wrong position 3. Signal/noise summing amplifier	1. Set S4 to correct position 2. Set S14 to OFF 3. Calibrate or replace: a. Card A3 for normal DIFAR NS b. Card A4 for normal DIFAR EW c. Card A5 for normal DIFAR OMNI, LOFAR and ALI LOFAR d. Card A6 for extended DIFAR NS e. Card A7 for extended DIFAR EW f. Card A8 for extended DIFAR OMNI, extended LOFAR and extended ALI LOFAR g. Card A9 for TRACK h. Card A2 for DL i. Card B18 for BITE
One target missing or wrong level in one or more modes	1. Oscillator board 2. Signal summing amplifier	1. Calibrate or replace oscillator (see Figure 5-1 for card vs. frequency) 2. Calibrate or replace signal summing amplifier (see Figure 5-1 for location)
Unable to select extended frequency band or normal frequency band: 1. all modes 2. one mode	1. Switch S13 2. Relay	1. Replace S13 2. a. LOFAR or ALI LOFAR: replace card B10 b. DIFAR EW: replace card B11 c. DIFAR NS: replace card B12 d. DIFAR OMNI: replace card B12

TABLE 6-3 (continued)

TARGET PROBLEMS (PASSIVE)

CONDITION	POSSIBLE CAUSE	ACTION REQUIRED
Unable to select extended frequency band or normal frequency band (continued) 3. BITE	3. a. Switch S1 b. Target generator	3. a. Replace S1 b. Replace card B19
TRACK target bearing incorrect	1. Bearing generator	1. Replace target bearing generator module
One or more target frequencies incorrect	1. Oscillator	1. Calibrate or replace oscillator (see Figure 5-1 for frequency vs. card)

TABLE 6-4

BITE PROBLEMS

CONDITION	POSSIBLE CAUSE	ACTION REQUIRED
Noise missing in all modes	1. S32 set to OFF 2. PRN generator 3. 900 KHz oscillator	1. Set S32 to ON 2. Replace card B15 3. Replace card B20
Noise missing from omni or sidebands	1. Noise filter	1. Replace card B16
Pilots missing or wrong level	1. Signal generator 2. Summing amplifier	1. Replace card B19 2. Replace card B17
One or more Targets missing, noise present	1. Target generator 2. Target summation	1. Replace card B19 2. Replace card B18
DEMON mode erroneous	1. Target generator 2. Target summation	1. Replace card B19 2. Replace card B18
DL Target missing	1. Target generator	1. Replace card B19
Sidebands missing	1. Modulator	1. Replace card B17
Omni missing	1. Modulator	1. Replace card B17

TABLE 6-5

COMPOSITE OUTPUT AND MISCELLANEOUS PROBLEMS
(PASSIVE)

CONDITION	POSSIBLE CAUSE	ACTION REQUIRED
System inoperative	1. Lack of power 2. S31 through S40 set to OFF	1. a. Check for hookup to an AC power source b. Check S1 of AC power panel for ON c. Check power supplies PS2 and PS5 for outputs 2. Set S31 through S40 to ON
One or more GRAM or OMNI Search outputs missing or wrong level	1. Switches S5 through S12 in wrong position 2. Output amplifier 3. Signal not being switched in	1. Set S5 through S12 to BITE for BITE mode or to SIMULATOR for other modes 2. Check output amplifier (see Figure 5-1 to determine which card) 3. Check relay card B6
System will not enter mode selected	1. Relays inoperative 2. DC power missing	1. a. Check power supply PS1 for output b. Check relay card B6 c. Check front panel switches 2. If BITE cannot be selected, check power supply PS4. PS4 also powers active section.
NS sidebands missing or wrong level	1. S33 set to OFF 2. Modulator driver 3. Modulator	1. Set S33 to ON 2. Calibrate or replace card B9 3. Replace card B7
EW sidebands missing or wrong level	1. S34 set to OFF 2. Modulator driver 3. Modulator	1. Set S34 to ON 2. Calibrate or replace card B9 3. Replace card B7
DEMON modulation not occurring or incorrect	1. Modulating signals not present or wrong level 2. Modulator	1. a. Check S31 for ON position b. Calibrate or replace oscillator cards (see Figure 5-1) 2. Replace card B13

TABLE 6-5

COMPOSITE OUTPUT AND MISCELLANEOUS PROBLEMS
(PASSIVE) continued

CONDITION	POSSIBLE CAUSE	ACTION REQUIRED
ASSG output missing or wrong level	1. ASSG not selected 2. Switches S5-S12 in BITE position 3. ASSG amplifier	1. Set S2 to ASSG 2. Set S5-S12 to SIMULATOR 3. Calibrate or replace card A10
Tracking Degrees readout not present, erratic or erroneous	1. Encoder 2. Display	1. Replace track bearing generator module 2. Replace display
6° alarm lamp fails to illuminate	1. Lamp burned out 2. Lamp driver 3. 6° pulse decoder	1. Replace lamp 2. Replace card C1 3. Replace card C2
Will not trigger remote track printer	1. 6° alarm circuit 2. 6° pulse decoder	1. Replace card C1 2. Replace card C2
TRACK composite output erroneous when remote input used; all or part missing or wrong level	1. S23 in LOCAL position 2. Remote track input source 3. Remote track input amplifier 4. Bad connection at input	1. Set S23 to REMOTE 2. Check remote signal source 3. Calibrate or replace card A10 4. Check J1 of front panel
Remote track output erroneous (normal output O.K.)	1. Output card	1. Replace card C1

TABLE 6-6

NOISE PROBLEMS (ACTIVE)

CONDITION	POSSIBLE CAUSE	ACTION REQUIRED
Noise not present in either Q47 or Q50	1. Switch S32 set to OFF 2. Noise not being generated 3. Filter defective	1. Set S32 to ON 2. a. Check PRN generator card B15 b. Check power supply PS4 3. Check filter card B20
Noise not present or wrong level in Q47 or Q50 CW, but is present in Q50 FM	1. Noise not being summed with signals 2. Improper resistance in noise line	1. Check signal/noise summing amplifier card C5 2. Calibrate card C5
Noise not present or wrong level in Q50 FM only	1. Noise not being summed with ramps 2. Improper resistance in noise line	1. Check signal/noise summing amplifier card C5 2. Calibrate card C5
Noise not present in Q47 only	1. Noise not being gated	1. a. Check target gate card C6 b. Check ping control card C8 c. Check gate control card C7
Noise not present in Q50 CW only 1. all ping widths	1. a. Noise not being summed with signals b. Noise not enabled	1. a. Check signal/noise summing amplifier card C5 b. Check ping control card C8 and gate control card C7
2. only one ping width	2. Noise not being gated	2. a. Check target gate card C6 b. Check gate control card C7 c. Check ping control card C8

TABLE 6-7

TARGET PROBLEMS (ACTIVE)

CONDITION	POSSIBLE CAUSE	ACTION REQUIRED
All targets missing in all modes, but noise is present	1. Switch S31 set to OFF 2. S19 and S20 set to NOISE ONLY	1. Set S31 to ON 2. Set S19 and S20 to SIGNAL + NOISE
One oscillator target frequency missing in both Q47 and Q50 CW	1. Target signal not being generated 2. Target signal not being gated in	1. Oscillator board defective (see Figure 5-1 for card number vs. frequency output) 2. a. Check relay card C13 b. Check signal summing amplifier card C5 c. Check target gate card C6 d. Check gate control card C7
One target yardage missing in all modes	1. Target yardage command not given 2. Target yardage command not followed	1. Check target time generator card C11 2. Check target time generator gate card C10
One target group missing in all modes	1. Target gate not operational 2. Improper gating	1. Check target gate card C6 2. a. Check relay card C13 b. Check gate control card C7 c. Check target time generator gate card C10
All FM ramps missing but targets present in CW	1. Ramp not being generated 2. Ramp not being gated	1. a. Check FM generator card C9 b. Check 2.42 MHz oscillator card B23 2. Check gate control card C7

TABLE 6-7

TARGET PROBLEMS (ACTIVE) (continued)

CONDITION	POSSIBLE CAUSE	ACTION REQUIRED
2.42 MHz occurring instead of a ramp: On ramp UP only or on ramp DOWN only	1. Modulating clock not functioning 2. Modulating signal not occurring	1. Check FM generator card C9 2. Check oscillator card B21
FM ramp occurs, but ramp characteristics are bad	1. Preset circuits not working	1. Check target time generator gate card C10
Only +40 or -40 ramps UP or DOWN occurring (1 of 4)	1. Preset not gated 2. Preset not accepted 3. Presets not generated	1. Check target time generator gates card C10 2. Check FM generator card C9 3. Check target time generator card C11
Ramps UP but not DOWN or ramps DOWN but not UP	1. UP or DOWN command not given/accepted	1. a. Check switch S27 b. Check FM generator card C9
FM level 1 ramp present, but not level 3 or level 3 present but not level 1 (see Table 4-3 for level vs. yardage)	1. Ramps not being gated	1. a. Check target gates card C6 b. Check gate control card C7
FM ramp not correct level	1. Improper impedance in circuit	1. Calibrate summing amplifier card C5
Ramp frequency incorrect 1. all ramps 2. +40 ramp only 3. -40 ramp only	1. Carrier frequency incorrect 2. Modulating frequency incorrect 3. Modulating frequency incorrect	1. Check 2.42 MHz oscillator card B23 2. Check 3.3875 KHz oscillator card B21 3. Check 2.9838 KHz oscillator card B21

TABLE 6-8

TIMING PROBLEMS (ACTIVE)

CONDITION	POSSIBLE CAUSE	ACTION REQUIRED
Targets occur at wrong yardage (time)	1. Base clock irregular 2. Time generator defective	1. Check 8.16 KHz oscillator card B23 2. Check target time generator card C11
Target ping widths wrong	1. Ping width generator defective	1. Check ping control card C8
FM generator timing is wrong	1. Base clocks are wrong 2. FM generator defective	1. Check 2.42 MHz 2,9838 Hz and 3,3875 Hz oscillator cards B23 and B21 2. Check FM generator card C9

TABLE 6-9

TOTAL OUTPUT AND MISCELLANEOUS PROBLEMS (ACTIVE)

CONDITION	POSSIBLE CAUSE	ACTION REQUIRED
Output not present in any Active mode, but AC power is ON	1. Switch S21 in wrong position 2. Start pulse not provided 3. DC power not present 4. Start pulse not accepted 5. Time base missing	1. Set S21 to REMOTE for external control or LOCAL for internal control 2. a. Depress S29 or S30 if in LOCAL control b. Check remote source for pulse c. Check receiver card C12 if REMOTE only 3. Check power supplies PS1, PS3, PS4, and PS6 4. Check target time generator card C11 5. Check 8.16 KHz oscillator card B23
Output on one range (A or B) missing or wrong level in all modes	1. Output amplifier	1. Check amplifier card C4 for an open or need of calibration
System will not enter mode selected: 1. Remote control 2. Local Control	 1. a. Will not accept mode commands b. Remote source defective 2. Switches S26, S27, or S28 defective	 1. a. Check receiver card C12 b. Check remote source 2. Check switches S26, S27, or S28 for proper operation

A1	~~BLANK~~ SCHEMATIC 14997 14998 SCHEMATIC SA1302
A2	DL MODE SCHEMATIC 14932
A3	SIGNAL SUMMING, NORMAL DIFAR NS SCHEMATIC 14965
A4	SIGNAL SUMMING, NORMAL DIFAR EW SCHEMATIC 14967
A5	SIGNAL SUMMING, NORMAL DIFAR OMNI, NORMAL LOFAR, NORMAL ALI LOFAR SCHEMATIC 14957
A6	SIGNAL SUMMING, EXTENDED DIFAR NS SCHEMATIC 14961
A7	SIGNAL SUMMING, EXTENDED DIFAR EW SCHEMATIC 14963
A8	SIGNAL SUMMING, EXTENDED DIFAR OMNI, EXTENDED LOFAR, EXTENDED ALI LOFAR SCHEMATIC 14955
A9	SIGNAL SUMMING, TRACK SCHEMATIC 14959
A10	REMOTE TRACK & ASSG SCHEMATIC 15017
A11	OSCILLATOR, 800 Hz & 2400 Hz SCHEMATIC 14998
A12	OSCILLATOR, 1325 Hz & 1700 Hz SCHEMATIC 15008
A13	OSCILLATOR, 607 Hz & 1280 Hz SCHEMATIC 15006
A14	OSCILLATOR, 615 Hz & 2050 Hz SCHEMATIC 15000
A15	OSCILLATOR, 600 Hz & 1200 Hz SCHEMATIC 14992
A16	OSCILLATOR, 95 Hz & 950 Hz SCHEMATIC 14994
A17	OSCILLATOR, 220 Hz & 245 Hz SCHEMATIC 15004
A18	OSCILLATOR, 195 Hz & 275 Hz SCHEMATIC 15002
A19	OSCILLATOR, 125 Hz & 1000 Hz SCHEMATIC 14990
A20	OSCILLATOR, 150 Hz & 300 Hz SCHEMATIC 14988
A21	OSCILLATOR, 80 Hz & 160 Hz SCHEMATIC 14986
A22	OSCILLATOR, 37.5 Hz & 75 Hz SCHEMATIC 14975
A23	OSCILLATOR, 2.5 Hz & 10 Hz SCHEMATIC 14973
A24	OSCILLATOR, 375 Hz & 750 Hz SCHEMATIC 14996
A25	BLANK

B1	BLANK TARGET GATE SCHEMATIC
B2	OUTPUT AMPLIFIER, GRAM I & II SCHEMATIC 15047
B3	OUTPUT AMPLIFIER, GRAM III & IV SCHEMATIC 15047
B4	OUTPUT AMPLIFIER, OMNI SEARCH I & II SCHEMATIC 15047
B5	OUTPUT AMPLIFIER, OMNI SEARCH III & IV SCHEMATIC 15047
B6	RELAY, PASSIVE SCHEMATIC 15023
B7	MODULATOR & SUMMATION SCHEMATIC 14929
B8	7.5 KHz & 15 KHz SIGNAL GENERATOR SCHEMATIC 14926
B9	MODULATOR DRIVER SCHEMATIC 14935
B10	SIGNAL + NOISE SUMMING, LOFAR & ALI LOFAR SCHEMATIC 14952
B11	SIGNAL + NOISE SUMMING, DIFAR EW, TRACK NS & TRACK EW SCHEMATIC 14950
B12	SIGNAL + NOISE SUMMING, DIFAR NS & DIFAR OMNI SCHEMATIC 14948
B13	DEMON INPUT AMPLIFIER, MODULATOR & OMNI NOISE FILTER SCHEMATIC 14938
B14	NOISE FILTERS, NS & EW SCHEMATIC 14944
B15	PSEUDORANDOM CODE GENERATOR SCHEMATIC 14860
B16	NOISE FILTER, BITE SCHEMATIC 14863
B17	MODULATOR & FILTER, BITE SCHEMATIC 14875
B18	TARGET SUMMATION, BITE SCHEMATIC 14872
B19	TARGET GENERATOR, BITE SCHEMATIC 14869
B20	OSCILLATOR, 900 KHz & ACTIVE FILTER SCHEMATIC 14866
B21	OSCILLATOR, 2.9838 KHz & 3.3875 KHz SCHEMATIC 14975
B22	OSCILLATOR, 26 KHz & 38 KHz SCHEMATIC 15014
B23	OSCILLATOR, 2.42 MHz & 8.16 KHz SCHEMATIC 14973

TRACK BEARING GENERATOR

C1	REMOTE TRACK OUTPUT SCHEMATIC 14978
C2	6° PULSE DECODER SCHEMATIC 15020
C3	~~BLANK~~
C4	OUTPUT AMPLIFIER, ACTIVE SCHEMATIC 15047
C5	SIGNAL + NOISE SUMMING, ACTIVE SCHEMATIC 14984
C6	TARGET GATES SCHEMATIC 14897
C7	GATE CONTROL SCHEMATIC 14888
C8	PING CONTROL SCHEMATIC 14894
C9	FM GENERATOR SCHEMATIC 14853
C10	TARGET TIME GENERATOR GATES SCHEMATIC 14891
C11	TARGET TIME GENERATOR SCHEMATIC 14885
C12	LINE RECEIVER SCHEMATIC 15037
C13	RELAY, ACTIVE SCHEMATIC 14970
C14	BLANK

P.C. CARD LOCATION
FIGURE 5-1

APPENDIX I

TECHNICAL MANUAL

For

TARGET BEARING ANGLE GENERATOR

BROWN ENGINEERING COMPANY, INC.

MODEL NO. 6802

This manual contains the information required for the maintenance of the Brown Engineering Model No. 6802 Target Bearing Angle Generator.

The unit consists of a motor, Vernitron P/N 18H6L-AA0-A0; an encoder Vernitron P/N VDE23-301-11; and a potentiometer, Vernitron P/N 49-60025. The motor has a 12,800:1 gearhead mounted to the front.

There is no scheduled maintenance required for the unit.

The information contained herein is supplied for isolating any malfunction. The components are of such a complexity that any failure necessitates replacement rather than repair.

Mechanical failure can only be produced by a violent blow to the unit. In such a case the damage will be visibly apparent. The symptom would be an inability of the unit to rotate. A check should be made of the gearhead housing and gears for bends, dents, etc. (see 01-60356).

Should the unit not rotate and no mechanical damage is evident, the following electrical tests should be performed:

1. Check pins 13 and 14 on the input connector to see that 115 volts, 60 hertz is being supplied to the unit.
2. Pin 13 on J1 should have two leads from the motor (white and red). With power disconnected, place an ohmmeter across pins 13 and 14 and see that the fixed phase of the motor is not open (see S01-60356). If the motor winding is open the motor must be replaced.
3. With power connected to the unit, read the voltage across the capacitor. The voltage should be 100 volts rms ±20 percent. If it is zero, the capacitor is shorted and must be replaced.

The above exhausts the possible causes for a rotation failure.

The bearing angle generator provides two outputs. The encoder produces a binary coded decimal signal from 0 to 359. Logic one is +5 volts dc, logic zero is 0 volt dc. The potentiometer provides two outputs. With an input reference voltage of V (1 volt rms to 3 volts rms, 10 hertz to 2400 hertz), the outputs are V sine θ and V cos θ, where θ is the potentiometer shaft position.

To examine either the encoder or potentiometer ouptut, the small gear on the gearhead should be removed. The gearhead has a ratio of 12,800:1; therefore, the torque at the motor shaft is multiplied by this factor at the output of the gearhead and the inertia is multiplied by the square of this number.

Should the encoder output fail completely, the +5 volts dc input should be checked. The white and black leads of the encoder should be examined for breaks. If this is not the problem, the encoder must be returned for repair.

A partial failure of the encoder may be verified by rotating the unit to the appropriate position (after the small gear has been removed) and by checking the levels of the output. Should the failure prove to be internal, the encoder must be replaced or returned for repair. A failure of the potentiometer sine-cosine output may be checked similarly. The input reference should be examined first. Then, leads and wiring should be inspected according to S01-60356. The potentiometer has a resistance of 10 kilohm per quadrant. This should be verified with an ohmmeter with power disconnected.

ZEROING

Should either the encoder or potentiometer be replaced in the

field, the unit must be rezerod. The following procedure is suggested:

1. Remove the small gear on the gearhead.
2. Tighten the coupling on the potentiometer. (Care should be taken not to overtighten or strip the screw.)
3. Tighten the clamp holding the large gear on the encoder shaft.
4. Loosen the clamp holding the coupling to the encoder shaft.
5. Energize the encoder (+5 volts dc) and the potentiometer.
6. Rotate the unit such that the potentiometer indicates a zero degree null (+0.25 degree).
7. Grasp the coupling with one hand and hold it fixed.
8. Rotate the encoder by gently moving the large gear until the encoder reading goes from 359 to 0.
9. Recheck the potentiometer null and encoder reading.
10. Tighten the clamp holding the coupling to the encoder shaft.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
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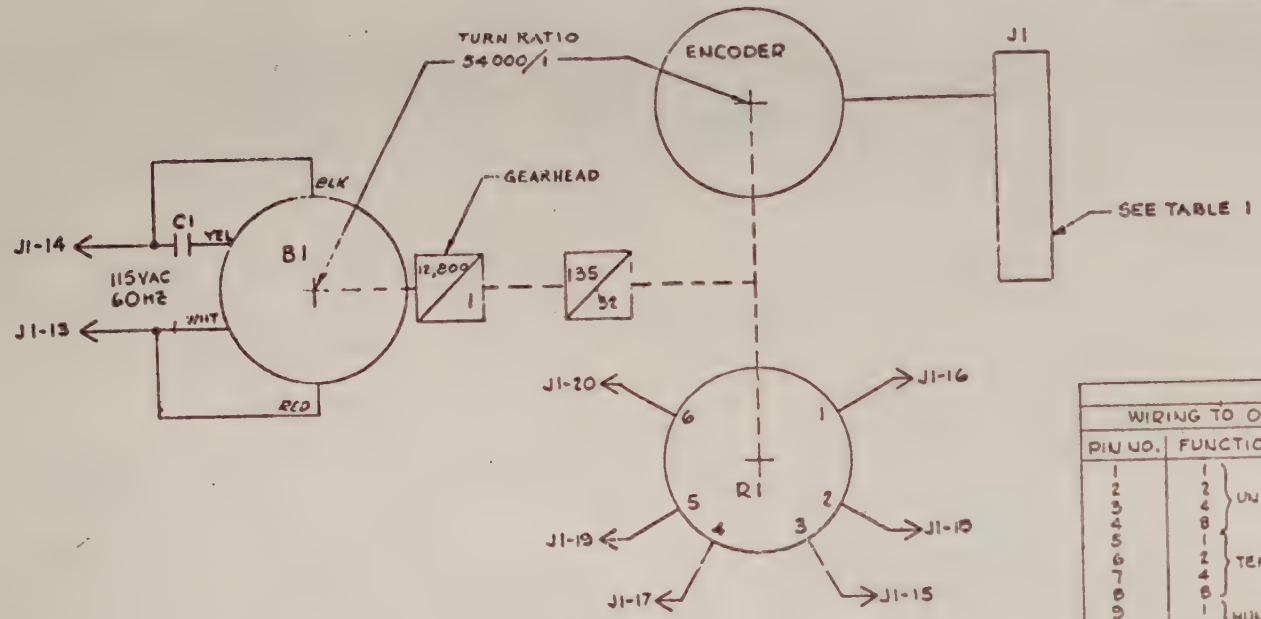
	D	[illegible]	[illegible]	[illegible]



NOTES:
1 ALL WIRES FROM R1 & B1 TO J1 TO BE #24AWG (GRAY)

TABLE 1
WIRING TO OUTPUT CONNECTOR J1 (ITT CANNON DB25P)

PIN NO.	FUNCTION	UNIT	LEAD OR TERMINAL
1	1	ENCODER	BROWN
2	2	UNITS	RED
3	4		ORANGE
4	8		YELLOW
5	1		GREEN
6	2	TENS	BLUE
7	4		VIOLET
8	8		GRAY
9	1	HUNDREDS	BROWN/WHITE
10	2		RED/WHITE
11	+5VDC		WHITE
12	+5V RETURN	ENCODER	BLACK
13	115VAC 60HZ HIGH	MOTOR	
14	115VAC 60HZ LOW	CAPACITOR (C1)	
15	+ SIGNAL	POTENTIOMETER (R1)	3
16	- SIGNAL		1
17	SIN OUTPUT		2
18	COS OUTPUT		4
19	0° TAP		5
20	180° TAP	POTENTIOMETER (R1)	6
21	SPARE		
22	SPARE		
23	SPARE		
24	SPARE		
25	SPARE		

HOLE DIAMETER	TOLERANCES
0135 THRU .125	+ .004 − .001
.126 THRU .250	+ .005 − .001
251 THRU .500	+ .006 − .001
501 THRU .750	+ .008 − .001
.751 THRU 1.000	+ .010 − .000

NEXT ASSY | USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES FRACTIONS ± 1/64
ANGLES ± 0° 30'
3 PLACE DECIMALS ± .005
2 PLACE DECIMALS ± .015

MATERIAL
NA

FINISH
NA

REMOVE ALL BURRS AND SHARP EDGES
DO NOT SCALE THIS DRAWING

CONTRACT NO.
451

DRAWN	[illegible]	2-7-69
CHECKED	[illegible]	[illegible] 69
APPROVED	[illegible]	[illegible]
APPROVED	[illegible]	[illegible]
RELEASE E.I.	[illegible]	

VERNITRON CORPORATION
DIGITAL PRODUCTS DIVISION
FARMINGDALE, NEW YORK

SCHEMATIC DIAGRAM

SIZE	CODE IDENT NO	DRAWING NO.	REV
C	30223	S01-60356	A

SCALE | WEIGHT | SHEET

S01-60356

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
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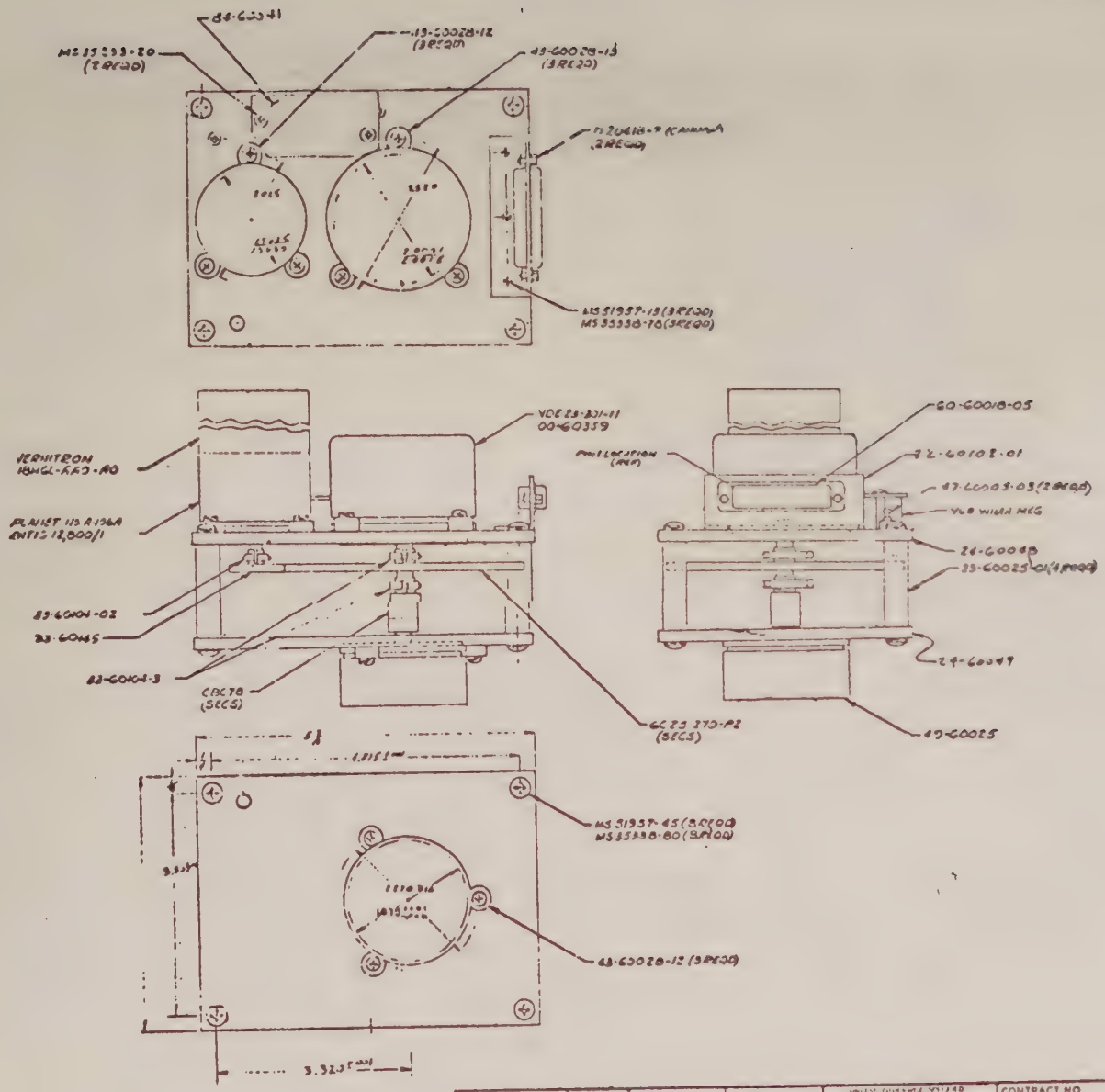


HOLE DIAMETER	TOLERANCES
.0135 THRU .125	+ .004 − .001
.126 THRU .250	+ .005 − .001
.251 THRU .500	+ .006 − .001
.501 THRU .750	+ .010 − .001

MATERIAL: N/A

FINISH: N/A

CONTRACT NO. 451

DRAWN	[illegible]	[illegible]
CHECKED	[illegible]	[illegible]
APPROVED	[illegible]	[illegible]
APPROVED	[illegible]	[illegible]
RELEASED	[illegible]	[illegible]

VERNITRON CORPORATION

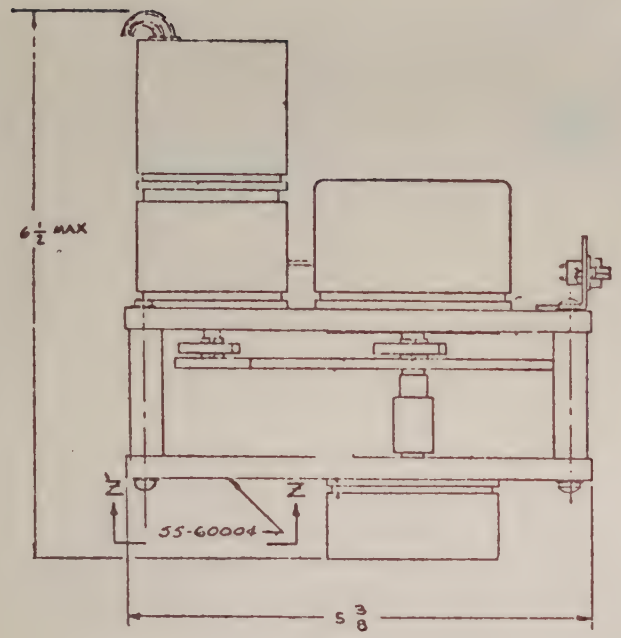
BEARING ANGLE GENERATOR

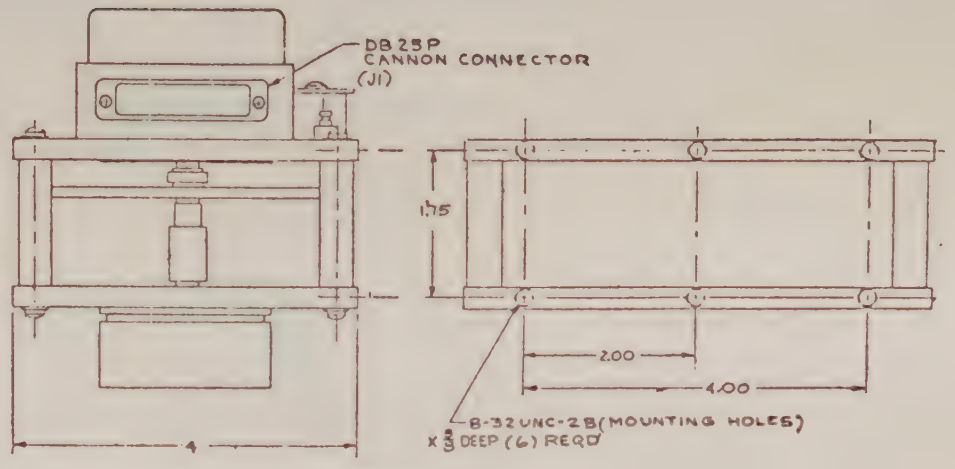
VCS102E

DRAWING NO

REV

PARTIAL VIEW Z-Z





NOTES:

1. OUTPUT: A) 10-LINE PARALLEL 1-2-4-8 BCD TO READ 0-359. LOGIC 1 = 5V ±10%; LOGIC 0 = 0V ± 5V LOGIC CIRCUIT IS DTL.
   B) POTENTIOMETER OUTPUT: $V_{sin\theta}$ & $V_{cos\theta}$, WHERE V = REFERENCE VOLTAGE & θ = ANGULAR SHAFT POSITION OF POTENTIOMETER
2. INPUT: A) 115V ±10V @ .1A, 60 ± 2 HZ
   B) +5VDC ±10% @ .2A
   C) POTENTIOMETER REFERENCE, 1VRMS-3VRMS 10HZ-2400HZ
3. ACCURACY: THE BEARING ANGLE REPRESENTED AT THE OUTPUT OF THE SINE-COSINE POTENTIOMETER SHALL BE WITHIN ±0.5 DEGREES, REFERENCED TO A CHANGE IN THE LEAST SIGNIFICANT BIT IN THE BCD OUTPUT FROM THE SHAFT POSITION ENCODER. THE BEARING ANGLE SHALL BE DEFINED AS THE ANGLE WHOSE TANGENT IS THE SINE OUTPUT DIVIDED BY THE COSINE OUTPUT.
4. SPEED: THE ENCODER & POTENTIOMETER SHALL BE DRIVEN AT A RATE OF 6 ± .05 DEGREES PER MINUTE.
5. LOAD: THE ACCURACY OF THE UNIT SHALL BE DEFINED FOR A LOAD OF 50K ±1% ON THE SINE & COSINE OUTPUTS OF THE POTENTIOMETER.
6. TEMPERATURE: THE UNIT SHALL OPERATE WITH THE ABOVE ACCURACY FROM +65°F TO 110°F. IT SHALL OPERATE WITHOUT DAMAGE FROM +110°F TO +120°F BUT SHALL NOT BE REQUIRED TO MEET THE ABOVE SPECIFICATIONS AT THE +110°F TO 120°F TEMPERATURE RANGE
7. MATING CONNECTOR FOR (J1) SUPPLIED WITH UNIT, No. DB25S CANNON

CONNECTOR (J1)

PIN	FUNCTION	
1	1	UNITS
2	2	
3	4	
4	8	
5	1	TENS
6	2	
7	4	
8	8	
9	1	HUNDREDS
10	-	
11	+5 VDC	POTENTIOMETER INPUT/OUTPUT
12	+5 V RETURN	
13	HI	115 V
14	LOW	60 HZ
15	+ SIGNAL	
16	- SIGNAL	
17	SIN OUTPUT	
18	COS OUTPUT	
19	0° TAP	
20	180° TAP	
21	SPARE	
22		
23		
24		
25		

INTERFACE CONTROL DRAWING

HOLE DIAMETER	TOLERANCES
.0135 THRU .125	+ .004 − .001
.126 THRU .250	+ .005 − .001
.251 THRU .500	+ .006 − .001
.501 THRU .750	+ .008 − .001
.751 THRU 1.000	+ .010 − .000

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: FRACTIONS ± 1/64
ANGLES ± 0° 30'
3 PLACE DECIMALS ± .005
2 PLACE DECIMALS ± .015

MATERIAL: NA

FINISH: NA

REMOVE ALL BURRS AND SHARP EDGES

DO NOT SCALE THIS DRAWING

CONTRACT NO. 151

DRAWN		
CHECKED	C.K.	
APPROVED		
APPROVED		
RELEASE EI 60-152		

VERNITRON CORPORATION
DIGITAL PRODUCTS DIVISION
FARMINGDALE, NEW YORK

BEARING ANGLE GENERATOR

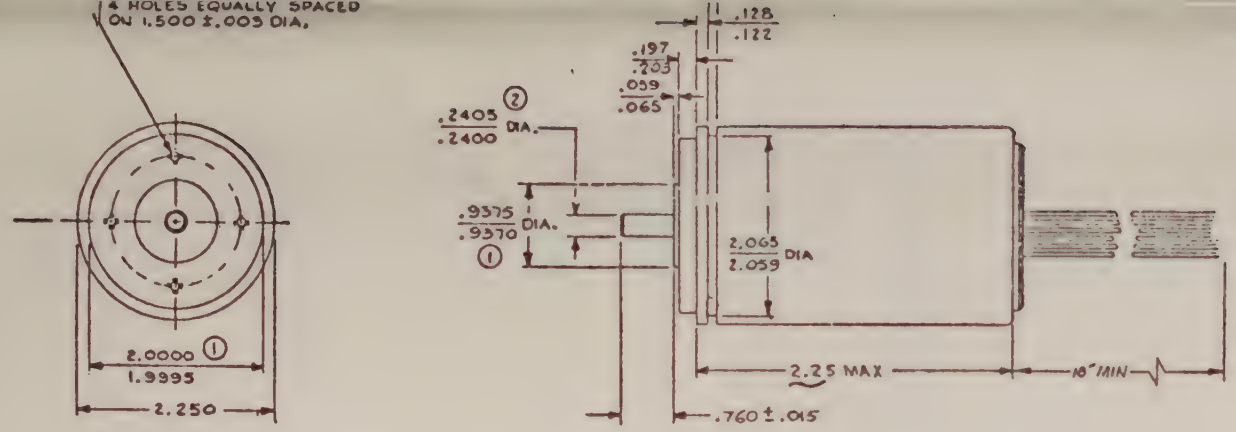
TYPE VCS108E

SIZE	CODE IDENT NO	DRAWING NO.	REV
C	30223	00-60356	F

SCALE | WEIGHT | SHEET

00-60356

CB CO 40-22 10147



PERFORMANCE CHARACTERISTICS

CODE	BCD 8421
SCAN	SELF SELECT
TOTAL COUNT	360
REVOLUTIONS FOR FULL COUNT	1
RESOLUTION PER REVOLUTION	1/360
STATIC ACCURACY	± 1/2 BIT
FRICTION TORQUE	50 GM. CM
INERTIA	30 GM. CM²
MAX. OPERATING SPEED	200 RPM
OPERATING LIFE (REVOLUTIONS)	6 X 10⁶
SAFE SPEED (MAX. MOMENTARY)	1500 RPM
ROTATION FOR INCREASING COUNT	C.W.

BINARY 1	+5 ± .5V
BINARY 0	0 ± .5V

CONNECTION	DECADE	LEAD COLOR
0 VOLTS + VOLTS		BLACK WHITE
1 2 4 8	1ST UNITS	BROWN RED ORANGE YELLOW
1 2 4 8	2ND TENS	GREEN BLUE VIOLET GRAY
1 2	3RD HUNDREDS	WHITE, BROWN WHITE, RED
INHIBIT (NOTE 7)		BLACK/WHITE

NOTES

1. OPERATING TEMPERATURE (DEGREES C) ____ -55 TO +85
2. WEIGHT (OUNCES) ____ 14
3. RUNOUT OF DIAMETERS ① (T.I.R. MAX.) ____ .001
4. RUNOUT OF DIAMETERS ② (T.I.R. MAX.) ____ .0008
5. END PLAY MEASURED WITH A REVERSING ONE POUND LOAD (MAX) ____ .0015
6. RADIAL PLAY MEASURED AS CLOSE TO THE BEARING AS POSSIBLE WITH A ONE POUND REVERSING LOAD APPLIED .12 INCH FROM END OF SHAFT. ____ .0008
7. SWITCHING INHIBIT TO GROUND WILL PREVENT SELECT CIRCUIT FROM CHANGING, INHIBIT TIME DEPENDS ON INPUT SHAFT SPEED.

INTERFACE CONTROL DRAWING

	NA		KINTRON
			LIT SELECT BCD ENCODER VUE 23-301-11
	NA		35000 · 00-60353 · SEL

APPLICATION		REVISIONS			
ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
	[illegible]				

POTENTIOMETER, SINE-COSINE

1. SCOPE

1.1 THIS SPECIFICATION COVERS THE DETAIL REQUIREMENTS FOR P/N 75-60025, SINE-COSINE POTENTIOMETER.

2. APPLICABLE DOCUMENTS

THE FOLLOWING DOCUMENT, OF THE ISSUE IN EFFECT ON DATE OF INVITATION FOR BIDS, FORMS A PART OF THIS SPECIFICATION TO THE EXTENT SPECIFIED HEREIN.

SPECIFICATIONS

MILITARY

MIL-R-39023, RESISTOR, VARIABLE, NON-WIREWOUND, PRECISION

SPECIFICATION CONTROL DRAWING

THERWISE SPECIFIED NS ARE IN INCHES ES; FRACTIONS ± 1/64 0° 30' ECIMALS ± .005 ECIMALS ± .015	CONTRACT NO. 451	VERNITRON CORPORATION DIGITAL PRODUCTS DIVISION FARMINGDALE, NEW YORK	
RIAL /A	DRAWN [illegible]	POTENTIOMETER SINE-COSINE	
	CHECKED [illegible]		
	APPD [illegible]		
	APPD [illegible]		
NH	RELEASE E.I. 69-165	SIZE A	CODE IDENT NO. 30223	DRAWING NO. 49-60025	REV
		SCALE	WEIGHT	SHEET 1 of 5	

3. REQUIREMENTS

3.1 LIFE EXPECTANCY

THE LIFE EXPECTANCY SHALL BE 4000 HOURS MINIMUM AT 1/60 RPM OVER THE OPERATING TEMPERATURE RANGE.

3.2 OPERATING TEMPERATURE

THE UNIT SHALL OPERATE AT THE REQUIRED ACCURACY FROM +65°F TO 100°F. IT MUST ALSO OPERATE FROM +110°F TO +120°F BUT SHALL NOT BE REQUIRED TO MEET THE ACCURACY REQUIREMENT.

3.3 ELECTRICAL CHARACTERISTICS

3.3.1 FUNCTION

THE OUTPUTS SHALL BE SINE AND COSINE SIGNALS.

3.3.2 ACCURACY

SIMULTANEOUS CONFORMITY SHALL BE ±0.15% PEAK TO PEAK.

3.3.3 POWER

THE UNITS SHALL OPERATE WITH AN APPLIED VOLTAGE OF ±3 VRMS MAX. 10 HZ TO 2400 HZ.

3.3.4 RESISTANCE

RESISTANCE SHALL BE 10K/QUAD ±10%.

3.3.5 DESIGN

THE UNIT SHALL HAVE SOLDER TERMINALS WIRED PER FIGURE I.

3.4 MECHANICAL

3.4.1 TORQUE

THE TORQUE SHALL BE 2 OZ.IN. MAX.

3.4.2 MECHANICAL ROTATION

MECHANICAL ROTATION SHALL BE 360° CONTINUOUS.

3.4.3 DIMENSIONS

PHYSICAL DIMENSIONS SHALL BE IN ACCORDANCE WITH FIGURE 2.

3.4.4 SMOOTHNESS

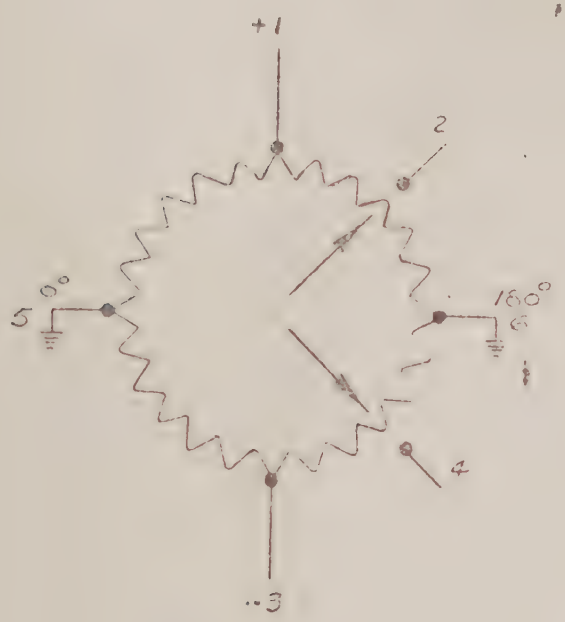
OUTPUT SMOOTHNESS SHALL BE IN ACCORDANCE WITH MIL-R-39023.

4. IDENTIFICATION

PART SHALL BE MARKED WITH VERNITRON PART NO. "30223 44-60025" IN .12 HIGH GOTHIC STYLE CHARACTERISTICS OF CONTRASTING COLOR.

SUGGESTED MANUFACTURERS

FAIRCHILD CONTROL, 225 PARK AVENUE, HICKSVILLE, NEW YORK.



SCHEMATIC

ROTATION CW FROM SHAFT END
WIPER NO. 2 - SINE
WIPER NO. 4 - COSINE

FIGURE I

SIZE	CODE IDENT NO	DRAWING NO	REV
A	30223	43-60025	
SCALE None	WEIGHT	SHEET 4 OF 5	

NOTES:

1. PILOT RUNOUT .001 MAX
2. SHAFT RUNOUT .001 MAX
3. LATERAL RUNOUT .003 MAX
4. AXIL SHAFT PLAY .005 MAX
5. RADIAL SHAFT PLAY .001 MAX.

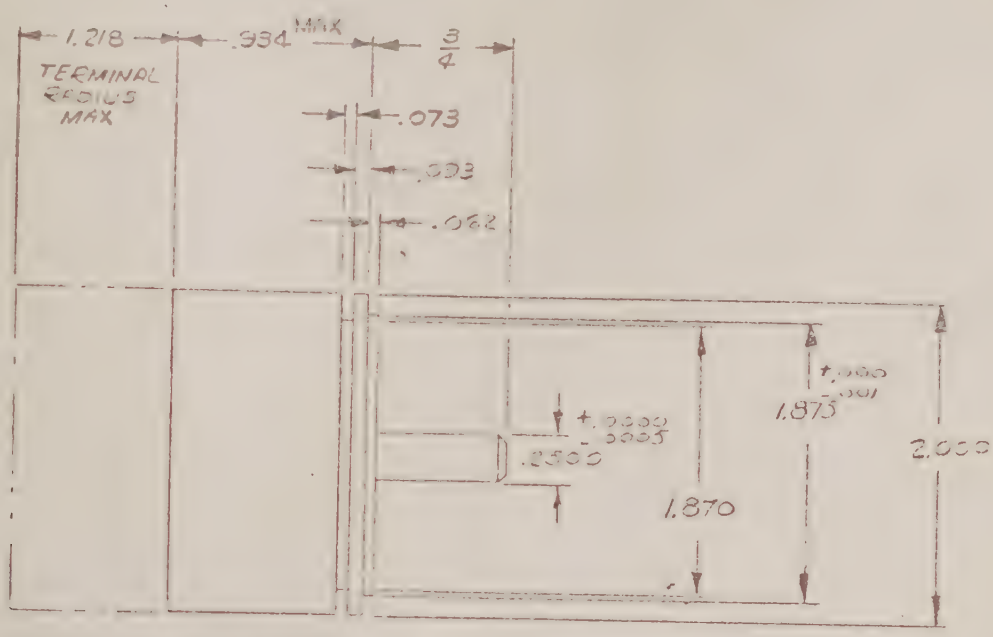


FIG 2A

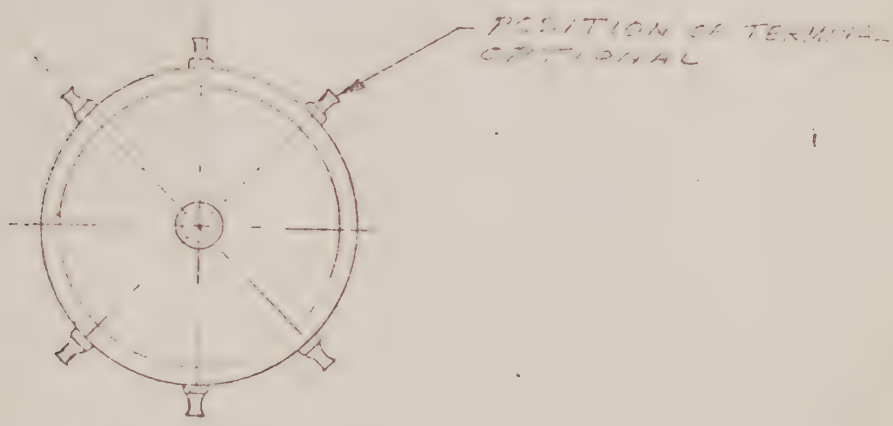


FIG 2B

FIGURE 2

SIZE	CODE IDENT NO.	DRAWING NO	REV
A	30223	49-60025	
SCALE NONE	WEIGHT	SHEET 5 OF 5	

APPENDIX II

CALIBRATION PROCEDURE

For

DIFAR SYSTEM SIMULATOR

CD-3800

1.0 INTRODUCTION

This document provides the procedures necessary to calibrate the DIFAR System Simulator CD-3800

1.1 CALIBRATION FREQUENCY

The DIFAR System Simulator is designed to operate within specification tolerances for a minimum of 336 consecutive hours (two weeks). The Simulator shall be tested at 336-hour intervals to determine if calibration is required.

1.2 CALIBRATION SEQUENCE

The procedures are written in the sequence that calibration is to be performed. Deviation from the sequence provided can result in erroneous calibration.

1.3 CALIBRATION ACCURACY

Tolerances for signals are specified in the calibration record.

1.4 EQUIPMENT WARMUP

The Simulator and support equipment should be turned on at least 30 minutes prior to starting calibration.

2.0 REQUIRED SUPPORT EQUIPMENT

All calibration shall be done with the Simulator connected to the Calibration Station SC-1046.

2.1 CALIBRATION STATION SC-1046

2.1.1 Test Demodulator CD-3801

2.1.2 Control Panel CD-3804

2.1.3 Frequency Synthesizer, General Radio 1161-A5

2.1.4 Oscilloscope, Tektronix R564B

2.1.4.1 Four Trace Plug-in, Tektronix 3A74

2.1.4.2 Time Base Unit, Tektronix 3B3

2.1.4.3 Differential Comparator Unit, Tektronix 3A7

2.1.5 RMS Voltmeter, Ballantine 323-01

2.1.6 Multifunction Meter Hewlett-Packard 3450A-001

2.1.7 Frequency Counter, Hewlett-Packard 5245L

2.1.8 Wave Analyzer, Hewlett-Packard 3590A

2.1.8.1 Sweeping Local Oscillator, Hewlett-Packard 3594A

2.1.9 Active Mode Switch Substitution Board

2.1.10 Variable Bearing Generator CD-3802

2.1.11 Jumpers

3.0 CALIBRATION OF POWER SUPPLY PANEL CD-3800-3

NOTE: Power Supply Panel CD-3800-3 must be installed in the DIFAR System Simulator CD-3800.

3.1 CALIBRATION PROCEDURE FOR DC OUPTUT VOLTAGE

3.1.1 Equipment Setup

3.1.1.1 Connect Multifunction Meter X Input LO to TB1-9 in Control Panel CD-3800-2. Input H1 connection is specified in 3.1.3.

3.1.2 Start of Test Conditions

3.1.2.1 MAIN POWER Switch on AC Power Control Board - ON

3.1.3 Detailed Calibration Procedure. Connect Multifunction Meters and make adjustments as specified in Table 3.1.1.

TABLE 3.1.1. DC OUTPUT VOLTAGE CALIBRATION

Paragraph	Motor x Inputs High	Motor x Inputs Low	Adjust	Voltage (Vdc)
3.1.3.1	TBI-1	TBI-9	PS2, Adj A	+15.0
3.1.3.2	TBI-2	TBI-9	PS2, Adj B	-15.0
3.1.3.3	TBI-4	TBI-9	PS5, Adj B	-15.0
3.1.3.4	TBI-5	TBI-9	PS5, Adj A	+15.0
3.1.3.5	TBI-6	TBI-9	PS1	+24.0
3.1.3.6	TBI-3	TBI-8	PS6	+5.0
3.1.3.7	TBI-7	TBI-8	PS4	+5.0
3.1.3.8	XA17-3	XA17-22	PS3	+5.0

4.0 CALIBRATION OF CONTROL PANEL CD-3800-2

NOTE: Control Panel CD-3800-2 must be installed in DIFAR System Simulator CD-3800.

4.1 CALIBRATION PROCEDURE FOR OSCILLATORS*

4.1.1 Equipment Setup

4.1.1.1 With the inputs in parallel, connect the oscilloscope, Multifunction Meter X Input, and the counter to OSC OUT Jack J2 through an isolation amplifier.

4.1.1.2 Install oscilloscope Differential Comparator 3A7 Plug-in.

4.1.2 Start of Test Conditions

4.1.2.1 Oscillator Switch S31 - OFF

4.1.3 Detailed Calibration Procedure

For each position of OSC Test Switch S24, make the adjustments specified in Table 4.1.1. Peak-to-peak voltage is to be measured using the oscilloscope, and voltage with the multifunction meter.

---

*The oscillator cards are nonrepairable subassemblies which must be replaced in the event of an oscillator malfunction. Filter circuits of each oscillator are individually tuned to achieve required accuracy and stability.

TABLE 4.1.1. OSCILLATOR FREQUENCY AND VOLTAGE CALIBRATION

Paragraph	S24	Adjust	Period/Frequency	Voltage
4.1.3.1	1	A23C11	400,000.0 μsec	-
4.1.3.2	1	A23R2	-	2.828 V Pk-Pk
4.1.3.3	2	Verify	100,000.0 μsec	-
4.1.3.4	2	A23R26	-	2.828 V Pk-Pk
4.1.3.5	3	A22C11	26,666.67 μsec	-
4.1.3.6	3	A22R2	-	2.828 V Pk-Pk
4.1.3.7	4	Verify	13,333.33 μsec	-
4.1.3.8	4	A22R26	-	1.000 V rms
4.1.3.9	5	A21C11	12,500.00 μsec	-
4.1.3.10	5	A21R2	-	1.00 V rms
4.1.3.11	6	A16C11	10,526.31 μsec	-
4.1.3.12	6	A16R2	-	1.000 V rms
4.1.3.13	7	A19C11	8,000.00 μsec	-
4.1.3.14	7	A19R2	-	1.000 V rms
4.1.3.15	8	A20C11	6,666.67 μsec	-
4.1.3.16	8	A20R2	-	1.000 V rms
4.1.3.17	9	Verify	6,250.00 μsec	-
4.1.3.18	9	A21R26	-	1.000 V rms
4.1.3.19	10	A18C3	5,128.20 μsec	-
4.1.3.20	10	A18R6	-	1.000 V rms
4.1.3.21	11	A17C3	4,545.45 μsec	-
4.1.3.22	11	A17R6	-	1.000 V rms
4.1.3.23	12	A17C15	4081.63 μsec	-
4.1.3.24	12	A17R30	-	1.000 V rms

TABLE 4.1.1. - Continued

Paragraph	S24	Adjust	Period/Frequency	Voltage
4.1.3.25	13	A18C15	3636.36 μsec	-
4.1.3.26	13	A18R30	-	1.000 V rms
4.1.3.27	14	Verify	333.33 μsec	-
4.1.3.28	14	A20R26	-	1.000 V rms
4.1.3.29	15	A24C11	2666.66 μsec	-
4.1.3.30	15	A24R2	-	1.000 V rms
4.1.3.31	16	A15C11	1666.66 μsec	-
4.1.3.32	16	A15R2	-	1.000 V rms
4.1.3.33	17	A13C3	1650.165 ~~1658.37~~ μsec	-
4.1.3.34	17	A13R6	-	1.000 V rms
4.1.3.35	18	A14C11	1639.344 ~~1626.01~~ μsec	-
4.1.3.36	18	A14R2	-	1.000 V rms
4.1.3.37	19	Verify	1333.33 μsec	-
4.1.3.38	19	A24R26	-	1.000 V rms
4.1.3.39	20	A11C11	1250.00 μsec	-
4.1.3.40	20	A11R2	-	1.000 V rms
4.1.3.41	21	Verify	1052.631 μsec	-
4.1.3.42	21	A16R26	-	1.000 V rms
4.1.3.43	22	Verify	1000,000 μsec	-
4.1.3.44	22	A19R26	-	1.000 V rms
4.1.3.45	23	Verify	833.333 μsec	-
4.1.3.46	23	A15R26	-	1.000 V rms
4.1.3.47	24	A13C11	781.250 μsec	-
4.1.3.48	24	A13R30	-	1.000 V rms

TABLE 4.1.1. - Concluded

Paragraph	S24	Adjust	Period/Frequency	Voltage
4.1.3.49	25	A12C3	754.716 μsec	-
4.1.3.50	25	A12R6	-	1.000 V rms
4.1.3.51	26	A12C15	588.235 μsec	-
4.1.3.52	26	A12R30	-	1.000 V rms
4.1.3.53	27	Verify	487.804 μsec	-
4.1.3.54	27	A14R26	-	1.000 V rms
4.1.3.55	28	Verify	416.666 μsec	-
4.1.3.56	28	A11R26	-	1.000 V rms
4.1.3.57	29	B21C3	335.143 μsec	-
4.1.3.58	29	Verify	-	4.5 V Pk-Pk min.
4.1.3.59	30	B21C9	295.202 μsec	-
4.1.3.60	30	Verify	-	4.5 V Pk-Pk min.
4.1.3.61	31	B23C3	122.549 μsec	-
4.1.3.62	31	Verify	-	3.8 V Pk-Pk min.
4.1.3.63	32	B8C4	15.0000 kHz	-
4.1.3.64	32	Verify	-	4.5 V Pk-Pk min.
4.1.3.65	33	B22C3	26.0000 kHz	-
4.1.3.66	33	B22R6	-	1.000 V rms
4.1.3.67	34	B22C15	38.0000 kHz	-
4.1.3.68	34	B22R30	-	1.000 V rms
4.1.3.69	35*	B23C8	2.420000 MHz	-
4.1.3.70	35	Verify	-	3 V Pk-Pk min.
4.1.3.71	36	A1C3	[illegible].836 μSec	—
4.1.3.72	36	A1R6	—	1.[illegible] Vrms

* Connect test equipment directly to J4, bypassing the isolation amplifier, for the 2.42-megahertz calibration.

4.1.3.73	37	A1C15	1,010.101 μSec	—
4.1.3.74	37	A1R30	—	1.000 Vrms

4.2 CALIBRATION PROCEDURE FOR NOISE SOURCES

4.2.1 Equipment Setup

4.2.1.1 Connect RMS Voltmeter to test points specified in 4.2.3.

4.2.2 Start of Test Conditions

4.2.2.1 S24 OSC TEST - OFF

4.2.2.2 S31 OSC - OFF

4.2.2.3 S32 NOISE - ON

S37 OMNI - ON

4.2.3 Detailed Calibration Procedure

Connect RMS Voltmeter and perform adjustments as specified in Table 4.2.1.

TABLE 4.2.1. NOISE

Paragraph	VM Inputs High	VM Inputs Low	Adjust	Voltage (V)
4.2.3.1	B13E2	B13E1	B13R26	0.603
4.2.3.2	B14E1	B13E1	B14R5	0.603
4.2.3.3	B14E3	B13E1	B14R27	0.603

4.3 CALIBRATION PROCEDURE FOR DEMON MODULATION

4.3.1 Equipment Setup

4.3.1.1 Install Differential Comparator 3A7 Plug-in.

4.3.1.2 Connect Oscilloscope input through an isolation amplifier to B13E2 - $\overline{\text{B13E1}}$.

4.3.1.3 Connect Frequency Synthesizer to B13E3 - $\overline{\text{B13E1}}$.

4.3.2 Start of Test Conditions

4.3.2.1 Set Frequency Synthesizer to 5,000 hertz, 2 volts rms output.

4.3.2.2 S24 OSC TEST - OFF

4.3.2.3 S31 OSC - OFF

4.3.2.4 S32 NOISE - OFF

4.3.2.5 S2 MODE - DEMON

4.3.3 Detailed Calibration Procedure

4.3.3.1 Measure peak-to-peak voltage.

4.3.3.2 Calculate 0.01 x (4.3.3.1) =

4.3.3.3 S24 OSC TEST - 4

4.3.3.4 Adjust B13R7 for peak-to-peak ripple equal to 4.3.3.2

4.3.3.5 S24 OSC TEST - 3

4.3.3.6 Verify peak-peak ripple to equal 4.3.3.2

4.3.3.7 S24 OSC TEST - 1

4.3.3.8 Verify peak-peak ripple to equal 4.3.3.2

4.4 CALIBRATION PROCEDURE FOR OUTPUT AMPLIFIER GAIN

4.4.1 Equipment Setup

4.4.1.1 Connect Frequency Synthesizer to B13E3 - $\overline{\text{B13E1}}$.

4.4.1.2 Connect Wave Analyzer through an isolation amplifier to B10E1 - $\overline{\text{B5E4}}$.

4.4.2 Start of Test Conditions

4.4.2.1 S24 OSC TEST - OFF

4.4.2.2 S31 OSC - OFF

4.4.2.3 S32 NOISE - OFF

4.4.2.4 S2 MODE - LOFAR

4.4.2.5 S5-8 DIFAR OUTPUTS - SIMULATOR

4.4.2.6 S9-12 OMNI SEARCH OUTPUTS - SIMULATOR

4.4.2.7 S14 CROSSTALK - OFF

4.4.2.8 S13 BANDWIDTH - NORM

4.4.2.9 Set Frequency Synthesizer to 5,000 hertz, 2 volts rms.

4.4.2.10 Set Wave Analyzer to 5,000 hertz, 100 hertz bandwidth.

4.4.3 Detailed Calibration Procedure

4.4.3.1 Adjust Wave Analyzer relative gain control for a reference of exactly 1.000.

4.4.3.2 Connect Wave Analyzer and make adjustments specified in Table 4.4.1.

TABLE 4.4.1. OUTPUT AMPLIFIER GAIN

Paragraph	Analyzer Inputs From CD-3804	Adjust	Relative Voltage (V)
4.4.3.3	J1	B4R7	8.000
4.4.3.4	J2	B4R20	8.000
4.4.3.5	J3	B5R7	8.000
4.4.3.6	J4	B5R20	8.000
4.4.3.7	J13	B2R7	8.000
4.4.3.8	J14	B2R20	8.000
4.4.3.9	J15	B3R7	8.000
4.4.3.10	J16	B3R20	8.000

4.5 CALIBRATION PROCEDURE FOR LOFAR, ALI LOFAR, and OMNI SIGNALS.

4.5.1 Equipment Setup

4.5.1.1 Connect Wave Analyzer through an isolation amplifier to test points specified in 4.5.3.

4.5.1.2 Remove Printed Circuit Card B8

4.5.2 Start of Test Conditions

4.5.2.1 S24 OSC TEST - 14

4.5.2.2 S31 OSC - OFF

4.5.2.3 S32 NOISE - OFF

4.5.2.4 S37 OMNI - ON

4.5.2.5 S33 NS - OFF

4.5.2.6 S34 EW - OFF

4.5.2.7 S2 MODE - DIFAR

4.5.2.8 S23 TRACK BEARING - LOCAL

4.5.2.9 Setup Variable Bearing Generator CD-3802 for a 1 000 hertz, +30 decibel S/N output.

4.5.2.10 S4 S/N LEVEL - 3

4.5.2.11 S14 CROSSTALK - OFF

4.5.3 Detailed Calibration Procedure

Perform adjustments specified in Table 4.5.1

4.5.3.41 Replace Printed Circuit Card B8

TABLE 4.5.1. LOFAR, ALI LOFAR, AND OMNI SIGNALS

Paragraph 4.5.3	S24	S13	S2	S4	Wave Analyzer Input	Frequency (Hz)	Adjust	Voltage (V)
.1	14	NORM	DIFAR	3	A5E4-$\overline{\text{B9E1}}$	300	A5R23	204.1
.2	12	NORM	TRACK	3	A9E2	245	A9R8	204.1
.3	12	NORM	TRACK	3	A9E1	245	A9R3	51.2
.4	14	NORM	DIFAR	3	CD-3804 J13	300	B9R6	66.2
.5	14	NORM	DIFAR	1	CD-3804 J13	300	B12R7	3.31
.6	14	EXT	DIFAR		CD-3804 J13	300	A8R5	66.2
.7	14	EXT	DIFAR		CD-3804 J13	300	B12R17	8.33
.8	14	EXT	ALI	3	CD-3804 J13	300	B10R31	8.33
.9	14	NORM	ALI	3	CD-3804 J13	300	B10R23	3.31
.10	14	NORM	LOFAR	3	CD-3804 J13	300	B10R7	5.26
.11	14	EXT	LOFAR	3	CD-3804 J13	300	B10R15	13.24
.12	2	NORM	DIFAR	3	CD-3804 J13	10	A5R1	66.2
.13	3	NORM	TRACK	3	CD-3804 J13	37.5	A9R6	66.2
.14	3	NORM	DIFAR	3	CD-3804 J13	37.5	A5R3	66.2
.15	5	NORM	DIFAR	3	CD-3804 J13	80	A5R5	66.2
.16	5	EXT	DIFAR	3	CD-3804 J13	80	A8R1	66.2
.17	6	NORM	DIFAR	3	CD-3804 J13	95	A5R7	66.2
.18	7	NORM	DIFAR	3	CD-3804 J13	125	A5R9	66.2
.19	8	NORM	DIFAR	3	CD-3804 J13	150	A5R11	66.2
.20	9	NORM	DIFAR	3	CD-3804 J13	160	A5R13	66.2
.21	10	NORM	DIFAR	3	CD-3804 J13	195	A5R15	66.2
.22	10	EXT	DIFAR	3	CD-3804 J13	195	A8R3	66.2
.23	11	NORM	DIFAR	3	CD-3804 J13	220	A5R17	66.2
.24	12	NORM	DIFAR	3	CD-3804 J13	245	A5R19	66.2
.25	12	NORM	TRACK	3	CD-3804 J13	245	A9R8	66.2
.26	13	NORM	DIFAR	3	CD-3804 J13	275	A5R21	66.2
.27	16	EXT	DIFAR	3	CD-3804 J13	600	A8R7	66.2
.28	20	EXT	DIFAR	3	CD-3804 J13	800	A8R9	66.2
.29	21	EXT	DL	3	CD-3804 J13	950	A2R20	467.0
.30	21	EXT	DL	2	CD-3804 J13	950	Verify	147.5
.31	21	EXT	DL	1	CD-3804 J13	950	Verify	46.7
.32	21	EXT	DIFAR	3	CD-3804 J13	950	A8R11	66.2

TABLE 4.5.1. - Continued

Paragraph 4.5.3	S24	S13	S2	S4	Wave Analyzer Input	Frequency (Hz)	Adjust	Voltage (V)
.33	23	EXT	DIFAR	3	CD-3804 J13	1200	A8R13	66.2
.34	24	EXT	DIFAR	3	CD-3804 J13	1280	A8R15	66.2
.35	25	EXT	DIFAR	3	CD-3804 J13	1325	A8R17	66.2
.36	26	EXT	DIFAR	3	CD-3804 J13	1700	A8R19	66.2
.37	27	EXT	TRACK	3	CD-3804 J13	2050	A9R10	66.2
.38	27	EXT	DIFAR	3	CD-3804 J13	2050	A8R21	66.2
.39	28	EXT	DIFAR	3	CD-3804 J13	2400	A8R23	66.2
.40	OFF	EXT	TRACK*	3	CD-3804 J13	1000	A10R3	66.2

* S23 Track Bearing - Remote

4.6 CALIBRATION PROCEDURE FOR LOFAR, ALI LOFAR, OMNI, DEMON NOISE

4.6.1 Equipment Setup

4.6.1.1 Connect RMS Voltmeter through an isolation amplifier to the CD-3804, J13.

4.6.1.2 Remove Printed Circuit Card B8

4.6.2 Start of Test Conditions

4.6.2.1 S24 OSC TEST - OFF

4.6.2.2 S31 OSC - OFF

4.6.2.3 S32 NOISE - ON

4.6.2.4 S37 OMNI - ON

4.6.2.5 S33 NS - OFF

4.6.2.6 S34 EW - OFF

4.6.2.7 S23 TRACK BEARING - LOCAL

4.6.2.8 S4 S/N LEVEL - 1

4.6.2.9 S2 MODE - LOFAR

4.6.2.10 S14 CROSSTALK - OFF

4.6.2.11 S13 BANDWIDTH - NORM

4.6.3 Detailed Calibration Procedure

Perform adjustments specified in Table 4.6.1

4.6.3.10 Replace Printed Circuit Card B8.

TABLE 4.6.1. LOFAR, ALI LOFAR, OMNI, AND DEMON NOISE

Paragraph 4.6.3	S2	S13	Adjust	Voltage (mV)
.1	LOFAR	NORM	B10R3	389
.2	LOFAR	EXT	B10R11	389
.3	ALI LOFAR	EXT	B10R27	389
.4	ALI LOFAR	NORM	B10R19	389
.5	DIFAR	NORM	B12R3	389
.6	DIFAR	EXT	B12R13	389
.7	DEMON	EXT	B12R13	389
.8	TRACK	EXT	A9R1	389
.9	DL	EXT	A2R31	389

4.7 CALIBRATION PROCEDURE FOR MODULATOR BALANCE AND GAIN

4.7.1 Equipment Setup

4.7.1.1 Connect Wave Analyzer input through an isolation amplifier to B7E2 - $\overline{\text{B7E3}}$.

4.7.2 Start of Test Conditions

4.7.2.1 S32 NOISE - OFF

4.7.2.2 S31 OSC - ON

4.7.2.3 S24 OSC TEST - OFF

4.7.2.4 S2 MODE - DL

4.7.2.5 S3 DL BEARING - 0°

4.7.2.6 S4 SN LEVEL - 3

4.7.2.7 S33 NS - ON

4.7.2.8 S34 EW - ON

4.7.2.9 S5 DIFAR OUTPUT GRAM I - SIMULATOR

4.7.2.10 Tune Wave Analyzer to 950 hertz, 100 hertz bandwidth.

4.7.3 Detailed Calibration Procedure

4.7.3.1 Adjust B9R17 for minimum 950 hertz signal.

4.7.3.2 S3 DL BEARING - 90°

4.7.3.3 Adjust B9R18 for minimum 950 hertz signal.

4.7.3.4 Connect isolated Wave Analyzer input to B9E5 - $\overline{\text{B9E1}}$.

4.7.3.5 Measure 950 hertz signal level.

4.7.3.6 Connect isolated Wave Analyzer input to B2E3 - $\overline{\text{B2E5}}$ and tune Wave Analyzer to 14.050 kilohertz.

4.7.3.7 Adjust B9R2 for 14.050 kilohertz signal level exactly equal to 950 hertz level measured in 4.7.3.5.

4.7.3.8 Connect isolated Wave Analyzer input to B9E4 - $\overline{\text{B9E1}}$ and tune Wave Analyzer to 950 hertz.

4.7.3.9 S3 DL BEARING - 0°

4.7.3.10 Measure 950 hertz signal level.

4.7.3.11 Connect isolated Wave Analyzer input to B2E3 - $\overline{\text{B2E5}}$ and tune Wave Analyzer to 14.050 kilohertz.

4.7.3.12 Adjust B9R1 for 14.050 kilohertz signal level exactly equal to 950 kilohertz level measured in 4.7.3.10.

4.8 CALIBRATION PROCEDURE FOR 7.5 AND 15 KILOHERTZ PILOTS AND DIFAR AND DL BEARING ALIGNMENT

4.8.1 Equipment Setup

4.8.1.1 Connect Wave Analyzer input through an isolation amplifier to the DIFAR GRAM II output CD-3804, J14.

4.8.1.2 Connect Multifunction Meter X Input to CD-3804, J11 (Test Demodulator EW output) and Y input to CD-3804, J10 (Test Demodulator NS output).

4.8.2 Start of Test Conditions

4.8.2.1 S2 MODE - DIFAR

4.8.2.2 S4 S/N LEVEL - 3

4.8.2.3 S5-8 DIFAR OUPTUTS - SIMULATOR

4.8.2.4 S13 BANDWIDTH - NORM

4.8.2.5 S14 CROSSTALK - OFF

4.8.2.6 S24 OSC TEST - 6

4.8.2.7 S31 OSC - OFF

4.8.2.8 S32 NOISE - OFF

4.8.2.9 S33 NS - ON

4.8.2.10 S34 EW - ON

4.8.2.11 S35 15 KHZ PILOT - ON

4.8.2.12 S36 7.5 KHZ PILOT - ON

4.8.2.13 Tune Wave Analyzer to 7.5 kilohertz, 10 hertz bandwidth.

4.8.2.14 Set up Test Demodulator to demodulate GRAM I signals.

4.8.2.15 Program Multifunction Meter for AC Ratio.

4.8.3 Detailed Calibration Procedure

4.8.3.1 Adjust B8R26 for 7.5 kilohertz pilot level of 1.60 volts rms.

4.8.3.2 Tune Wave Analyzer to 15 kilohertz.

4.8.3.3 Adjust B7R25 for 15 kilohertz pilot level of 1.60 volts rms.

4.8.3.4 Connect isolated Wave Analyzer input to the Test Demodulator NS ouptut and tune Wave Analyzer to 95 hertz.

4.8.3.5 Adjust the Test Demodulator phase controls for a condition of minimum 95 hertz signal form the NS ouptut and the phase sense lamp illuminated.

4.8.3.6 Adjust the 15 kilohertz pilot phase B8R27 for zero on the Test Demodulator Phase Meter, with the Meter Sensitivity switch in X1.

4.8.3.7 Connect isolated Wave Analyzer input to DIFAR GRAM II output.

4.8.3.8 Position controls and perform adjustments specified in Table 4.8.1. The output voltage for each step, as indicated by the Wave Analyzer, shall be 51.2 millivolts.

TABLE 4.8.1. NORMAL DIFAR DIRECTIONAL SIGNALS, LEVEL 3

Paragraph 4.8.3	S24	Multifunction Meter Input	Multifunction Meter Ratio	Analyzer Frequency (kHz)	Adjust EW	Adjust NS
.9	2	-	-	14.990	-	A3R11
.10	3	Front	0.5774	14.963	A4R17	A3R13
.11	5	Front	1.000	14.920	A4R15	A3R15
.12	6	-	-	14.905	A4R11	-
.13	7	Rear	0.5774	14.875	A4R13	A3R1
.14	8	Rear	1.000	14.850	A4R19	A3R3
.15	9	-	-	14.840	-	A3R5
.16	10	Front	0.5774	14.805	A4R1	A3R7
.17	11	Front	1.000	14.780	A4R3	A3R9
.18	12	-	-	14.755	A4R5	-
.19	13	Rear	0.5774	14.725	A4R7	A3R17
.20	14	Rear	1.000	14.700	A4R9	A3R19

4.8.3.21 S13 Bandwidth - EXT

4.8.3.22 Position controls and perform adjustments specified in Table 4.8.2. The output voltage for each step, as indicated by the Wave Analyzer, shall be 51.2 millivolts.

TABLE 4.8.2. EXTENDED DIFAR DIRECTIONAL SIGNALS, LEVEL 3

Paragraph 4.8.3	S24	Multifunction Meter Input	Multifunction Meter Ratio	Analyzer Frequency (kHz)	Adjust EW	Adjust NS
.23	5	-	-	14.920	-	A6R11
.24	10	Front	0.5774	14.805	A7R17	A6R13
.25	14	Front	1.000	14.700	A7R15	A6R15
.26	16	-	-	14.400	A7R11	-
.27	20	Rear	0.5774	14.200	A7R13	A6R1
.28	21	Rear	1.000	14.050	A7R19	A6R3
.29	23	-	-	13.800	-	A6R5
.30	24	Front	0.5774	13.720	A7R1	A6R7
.31	25	Front	1.000	13.675	A7R3	A6R9
.32	26	-	-	13.300	A7R5	-
.33	27	Rear	0.5774	12.950	A7R7	A6R17
.34	28	Rear	1.000	12.600	A7R9	A6R19

4.8.3.35 S4 S/N Ratio - 1

4.8.3.36 Connect isolated Wave Analyzer input to CD-3804 as specified in Table 8.3.3 and make required adjustments until all conditions are met.

TABLE 4.8.3. EXTENDED AND NORMAL DIFAR DIRECTIONAL SIGNALS, LEVEL 1

Paragraph 4.8.3	S24	S13	Input	Wave Analyzer Frequency	Level	Adjust EW	Adjust NS
.37	5	NORM	J14	14.920 kHz	2.56 mV	B11R7	B12R27
.38	5	NORM	J11	80 Hz	=4.8.3.38	B11R7	-
.39	5	NORM	J10	80 Hz	=4.8.3.37	-	B12R27
.40	21	EXT	J14	14.050 kHz	6.45 mV	B11R17	B12R37
.41	21	EXT	J11	950 Hz	=4.8.3.41	B11R17	-
.42	21	EXT	J10	950 Hz	=4.8.3.40	-	B12R37

4.8.3.43 S2 Mode - DL

4.8.3.44 S4 S/N Level - 3

4.8.3.45 S24 OSC Test - 21

4.8.3.46 Connect isolated Wave Analyzer input to CD-3804, J14.

4.8.3.47 Tune Wave Analyzer to 14.050 kilohertz

4.8.3.48 Set Multifunction Meter Input switch to REAR.

4.8.3.49 Position controls and perform adjustments specified in Table 4.8.4.

TABLE 4.8.4. DL DIRECTIONAL SIGNALS, LEVEL 3

Paragraph 4.8.3	S3 (deg)	Ratio	14.050 kHz Level (mV)	Adjust EW	Adjust NS
.50	0	-	362	-	A2R22
.51	90	-	362	A2R26	-
.52	45	1.000	362	A2R27	A2R23
.53	135	1.000	362	-	A2R25
.54	315	1.000	362	A2R29	-

4.9 CALIBRATION PROCEDURE FOR TRACK BEARING ALIGNMENT

4.9.1 Equipment Setup

4.9.1.1 Connect Multifunction Meter X Input to A9E2 - $\overline{\text{B9E1}}$ and Y Input to A9E3 - $\overline{\text{B9E1}}$.

4.9.1.2 Connect Wave Analyzer input through an isolation amplifier to the DIFAR GRAM II output CD-3804, J14.

4.9.2 Start of Test Conditions

4.9.2.1 F1 FUSE - Remove

4.9.2.2 S2 MODE - TRACK

4.9.2.3 S5-8 DIFAR OUTPUTS - SIMULATOR

4.9.2.4 S14 CROSSTALK - OFF

4.9.2.5 S23 TRACK BEARING - LOCAL

4.9.2.6 S24 OSC TEST - 12

4.9.2.7 S31 OSC - OFF

4.9.2.8 S32 NOISE - OFF

4.9.2.9 S33 NS - ON

4.9.2.10 S34 EW - ON

4.9.2.11 S35 15 KHZ PILOT - ON

4.9.2.12 S36 7.5 KHZ PILOT - ON

4.9.2.13 Set up Test Demodulator to demodulate GRAM I signals.

4.9.2.14 Program Multifunction Meter for AC Ratio.

4.9.2.15 Tune Wave Analyzer to 14.755 kilohertz, 10 hertz bandwidth.

4.9.2.16 Set Variable Bearing Generator CD-3802 for [illegible] hertz, 45 degrees, +30 decibel S/N Ratio, GR1161 for 245 hertz.

4.9.3 Detailed Calibration Procedure

4.9.3.1 Adjust A9R5 for a ratio of 1.000.

4.9.3.2 Set Multifunction Meter Input switch to REAR.

4.9.3.3 Set TRACK BEARING to 45, 135, 225, or 315 degrees by inserting fuse F1 until desired bearing is indicated by the track bearing readout.

4.9.3.4 Adjust B11R27 (NS) and B11R35 (EW) for a ratio of 1.000 and a 14.755 kilohertz signal level of 51.2 millivolts.

4.9.3.5 S23 TRACK BEARING - REMOTE

4.9.3.6 Adjust A10R11 (NS) and A10R19 (EW) for a ratio of 1.000 and a 14.755 kilohertz signal level of 51.2 millivolts.

4.9.3.5 S23 TRACK BEARING - REMOTE

4.9.3.6 Adjust A10R11 (NS) and A10R19 (EW) for a ratio of 1.000 and a 14.755 kilohertz signal level of 51.2 millivolts.

4.10 CALIBRATION PROCEDURE FOR DIRECTIONAL NOISE LEVEL

4.10.1 Equipment Setup

4.10.1.1 Connect RMS Voltmeter to B9E4 - $\overline{\text{B9E1}}$.

4.10.2 Start of Test Conditions

4.10.2.1 S2 MODE - DIFAR

4.10.2.2 S13 BANDWIDTH - NORMAL

4.10.2.3 S24 OSC TEST - OFF

4.10.2.4 S23 TRACK BEARING - LOCAL

4.10.2.5 S31 OSC - OFF

4.10.2.6 S32 NOISE - ON

4.10.2.7 S37 OMNI - ON

4.10.3 Detailed Calibration Procedure

4.10.3.1 Connect RMS voltmeter and adjust potentiometers for an rms noise level of 302 millivolts.

4.10.3.2 Position controls and perform adjustments specified in Table 4.10.1.

TABLE 4.10.1. DIRECTIONAL NOISE

Paragraph 4.10.3	S2	S13	RMS Voltmeter Input High	RMS Voltmeter Input Low	Adjust
.2	DIFAR	NORM	B9E4	B9E1	B12R23
.3	DIFAR	EXT	B9E4	B9E1	B12R33
.4	TRACK	EXT	B9E4	B9E1	B11R23
.5	DL	EXT	B9E4	B9E1	A2R37
.6	DIFAR	EXT	B9E5	B9E1	B11R13
.7	DIFAR	NORM	B9E5	B9E1	B11R3
.8	TRACK	NORM	B9E5	B9E1	B11R31
.9	DL	NORM	B9E5	B9E1	A2R43

4.11 CALIBRATION PROCEDURE FOR BITE AND ASSG AMPLIFIER

4.11.1 Equipment Setup

4.11.1.1 Connect Wave Analyzer input through an isolation amplifier to B18E5 - $\overline{\text{B18E1}}$.

4.11.2 Start of Test Conditions

4.11.2.1 S1 BITE - DL

4.11.2.2 S2 MODE - BITE

4.11.2.3 S5-12 OUTPUTS - BITE

4.11.2.4 S32 NOISE - OFF

4.11.2.5 S38 PILOT - ON

4.11.2.6 Tune Wave Analyzer to 1875 hertz, 10 hertz bandwidth.

4.11.2.8 Set up Test Demodulator to demodulate GRAM I signals.

4.11.3 Detailed Calibration Procedure

4.11.3.1 Measure 1,875 hertz signal level and record reading.

4.11.3.2 Connect isolated Wave Analyzer input to B18E7 - $\overline{\text{B18E1}}$.

4.11.3.3 Adjust B18R1 for an 1,875 hertz signal level identical to that measured in 4.11.3.1.

4.11.3.4 Connect Wave Analyzer input to Test Demodulator NS output, CD-3804, J10.

4.11.3.5 Place a jumper between B17E1 and B17E2.

4.11.3.6 Adjust the Test Demodulator phase controls for a condition of minimum 1,875 hertz signal from the NS output and the Phase Sense lamp illuminated.

(POT TOWARD REAR)

4.11.3.7 Adjust the 15 kilohertz pilot phase B17R23 for zero on the Test Demodulator Phase Meter, with the Meter Sensitivity switch in X1.

4.11.3.8 Remove jumper.

4.11.3.9 Measure 1,875 hertz signal level and record reading.

4.11.3.10 Connect Wave Analyzer input to Test Demodulator EW output, CD-3804, J11.

4.11.3.11 Adjust B17R63 for an 1,875 hertz signal level identical to that measured in 4.11.3.9.

4.11.3.12 Connect isolated Wave Analyzer input to CD-3804, J13 and Tune Wave Analyzer to 7.5 kilohertz.

4.11.3.13 Measure 7.5 kilohertz signal level.

4.11.3.14 S2 MODE - ASSG

4.11.3.15 Adjust A10R27 for a 7.5 kilohertz signal level identical to that measured in 4.11.3.13.

4.12 CALIBRATION PROCEDURE FOR ACTIVE MODE

4.12.1 Equipment Setup

4.12.1.1 Connect RMS Voltmeter to CD-3804, J6, Active Audio, Range B.

4.12.1.2 Remove Board C6 and install Switch Substitution Board in location C6.

4.12.2 Start of Test Conditions

4.12.2.1 S15 PING FREQ - 26 KHZ

4.12.2.2 S16 ZERO DOPPLER - 750 HZ

4.12.2.3 S17 PING - A OR B

4.12.2.4 S18 B PING - ZERO DELAY

4.12.2.5 S19 RANGE A - NOISE ONLY

4.12.2.6 S20 RANGE B - NOISE ONLY

4.12.2.7 S21 MODE CONTROL - LOCAL

4.12.2.8 S22 PING CONTROL - MANUAL

4.12.2.9 S24 OSC TEST - OFF

4.12.2.10 S25 PING WIDTH - 0.1

4.12.2.11 S26 CASS - CW

4.12.2.12 S27 FM - DOWN

4.12.2.13 S28 BUOY - Q47

4.12.2.14 S31 OSC - OFF

4.12.2.15 S32 NOISE - ON

4.12.2.16 S37 OMNI - ON

4.12.2.17 TS1 - 15 - OFF

4.12.3 Detailed Calibration Procedure

4.12.3.1 Adjust active mode noise levels in accordance with Table 4.12.1.

TABLE 4.12.1. ACTIVE MODE NOISE

Paragraph 4.12.3	S19 and S20	S25	S26	S28	RMS VM Input CD-3804	Test Switch On*	Adjust	Noise Voltage
.2	Noise Only	0.1	CW	Q47	J6	None	C4R7	0.10 V rms
.3	Noise Only	0.1	CW	Q47	J5	None	C4R20	0.10 V rms
.4	Signal + Noise	0.1	CW	Q47	J5	TS11-1	C5R17	32 mV rms
.5	Signal + Noise	0.1	CW	Q50	J5	TS4-5	C5R19	32 mV rms
.6	Signal +Noise	0.5	CW	Q50	J5	TS12-11	C5R11	71.7 mV rms
.7	Signal + Noise	1.0	CW	Q50	J5	TS5-15	C5R13	100 mV rms
.8	Signal + Noise	1.0	FM	Q50	J5	TS5-15	C5R27	100 mV rms

*All other switches on the Switch Substitution Board OFF.

4.12.3.9 Return all switches to the respective positions specified in 4.12.2.

4.12.3.10 S19-20 Range A and B - Signal and Noise

4.12.3.11 S32 Noise - Off

4.12.3.12 S31 OSC - On.

4.12.3.13 Connect ~~RMS Vol meter~~ (WAVE ANALYZER) to CD-3804, J5

4.12.3.14 Adjust active mode target levels in accordance with Table 4.12.2.

TABLE 4.12.2. Active Mode Targets

Paragraph 4.12.3	Test Switch On*	S28	S26	Adjust	Signal Level
.15	A-- TS8-606HZ	Q47	CASS	C5R1	84.3 mV rms
.16	C-- TS1-606HZ	Q47	CASS	C5R3	84.3 mV rms
.17	6-- TS2-610HZ	Q47	CASS	C5R5	84.3 mV rms
.18	17- TS13-750HZ	Q47	CASS	C5R7	150 mV rms
.19	X- TS14 26KHZ	Q47	CASS	C5R9	1.0 V rms
.20	F-- TS9 375HZ	Q47	CASS	C5R21	15.0 mV rms
.21	K-- TS10 990 HZ	Q47	CASS	C5R23	15.0 mV rms
.22	N-- TS3 990 HZ	Q47	CASS	C5R25	84.3 mV rms
.23	U-- TS6-950HZ	Q50	CASS	C5R15	37.8 mV rms
.24 +	18-- TS7-800HZ	Q50	FM	C5R29	~~21.1~~ 26.6 mV ~~rms~~ ON WAVE ANAL.
.25 +	20- TS15-800HZ	Q50	FM	C5R32	~~119~~ 141 mV ~~rms~~ ON WAVE ANAL.

*All other switches on the Switch Substitution Board OFF.

4.12.3.26 Remove Switch Substitution Board and replace board C6.

+ S31 OFF
S24 TO 35
S22 TO MANUAL
SHORT C9E2 TO B2E4
PUSH S29 ONCE AND RELEASE
TUNE WAVE ANALYZER TO 800 HZ

5.0 CALIBRATION RECORD

The following data sheets are to be used to record the periodic calibration data.

FREQUENCY LIBRATION

LIMIT		NOMINAL		UPPER	
PERIOD MS		FREQ HZ	PERIOD W		PER
04,040	04			5	16,039
00,250	27	10.0	100,000.000	5	9,750
6,684	56	37.5	26,666.667	5	16,648
7	79	75.0	13,333.333	5	3,328.[illegible]
	17	80.0	12,500.000		2,496.095
	17		10,526.316		0,523.546
			8000.000	5	7998.400
67	78		6666.667		6665.556
5	77		6250.000	5	6249.024
2	33		5128.205	5	5127.548
4			4545.455	5	4544.938
40	49	24.0	4081.6[illegible]	5	4081.216
363	34	27.0	363[illegible]	275.125	3636.033
33	1	30.0	333[illegible].333	5[illegible].125	3333.[illegible]56
26		375.0	266[illegible]	375.2	2665.245
16	22	60.0	1666.667	[illegible].2	1666.111
1650.715		606.0	1[illegible]		649.615
163[illegible].546		60.0	1639.316	615.2	1638.78[illegible]
1333	81	750.0	1333.333	750.2	1332.978
125		800.0	1250.000	800.2	1249.688
1052		950.0	1052.632	950.2	1052.410
1000		1000.0	1000.000	1000.2	9[illegible]9.200
93[illegible]		12[illegible]	833.333	1200.2	8[illegible]3.194
78[illegible]		2[illegible].0	781.250	1280.2	781.128
754		13[illegible].0	754.717	1325.2	754.603
58[illegible]		17[illegible].0	588.235	1700.2	588.166
49[illegible]		[illegible]	487.805	2050.2	487.757
		[illegible]	41[illegible]		416.632
		[illegible]8	3[illegible]		335.12[illegible]
		[illegible]5	[illegible]		295.18[illegible]
		[illegible]	122.549		122.42[illegible]
		K			
		K			
		K			
		M			

CALIBRATION FOR TEST PANEL CD-3800

Date _____

Serial No. _____

Project AN/AQA-7(V)

Paragraph	Description	Recorded Data		
		L.L.	Test Data	U.L.
4.1.3.25	275 Hz Period	3,636.29 μsec		3,636.42 μsec
4.1.3.26	275 Hz Voltage	0.988 V		1.012 V
4.1.3.27	300 Hz Period	3,333.26 μsec		3,333.40 μsec
4.1.3.28	300 Hz Voltage	0.988 V		1.012 V
4.1.3.29	375 Hz Period	2,666.61 μsec		2,666.71 μsec
4.1.3.30	375 Hz Voltage	0.988 V		1.012 V
4.1.3.31	600 Hz Period	1,666.63 μsec		1,666.69 μsec
4.1.3.32	600 Hz Voltage	0.988 V		1.012 V
4.1.3.33	60~~3~~6 Hz Period	1,6~~50~~49.665 ~~.34~~ μsec		1,65~~8~~.665 ~~.40~~ μsec
4.1.3.34	60~~3~~6 Hz Voltage	0.988 V		1.012 V
4.1.3.35	61~~5~~0 Hz Period	1,6~~25~~38.844 ~~.98~~ μsec		1,6~~26~~39.844 ~~.04~~ μsec
4.1.3.36	61~~5~~0 Hz Voltage	0.988 V		1.012 V
4.1.3.37	750 Hz Period	1,333.30 μsec		1,333.36 μsec
4.1.3.38	750 Hz Voltage	0.988 V		1.012 V
4.1.3.39	800 Hz Period	1,249.97 μsec		1,250.03 μsec
4.1.3.40	800 Hz Voltage	0.988 V		1.012 V
4.1.3.41	950 Hz Period	1,052.610 μsec		1,052.652 μsec
4.1.3.42	950 Hz Voltage	0.988 V		1.012 V
4.1.3.43	1,000 Hz Period	999.980 μsec		1,000.020 μsec
4.1.3.44	1,000 Hz Voltage	0.988 V		1.012 V
4.1.3.45	1,200 Hz Period	833.316 μsec		833.350 μsec
4.1.3.46	1,200 Hz Voltage	0.988 V		1.012 V
4.1.3.47	1,280 Hz Period	781.235 μsec		781.265 μsec
4.1.3.48	1,280 Hz Voltage	0.988 V		1.012 V
4.1.3.49	1,325 Hz Period	754.701 μsec		754.731 μsec
4.1.3.50	1,325 Hz Voltage	0.988 V		1.012 V
4.1.3.51	1,700 Hz Period	588.213 μsec		588.247 μsec
4.1.3.52	1,700 Hz Voltage	0.988 V		1.012 V
4.1.3.53	2,050 Hz Period	487.794 μsec		487.814 μsec
4.1.3.54	2,050 Hz Voltage	0.988 V		1.012 V
4.1.3.55	2,400 Hz Period	416.658 μsec		416.674 μsec
4.1.3.71	994 Hz Period	1,005.836 μSec		1,006.236 μSec
[illegible]	994 Hz Voltage	0.988 V		1.012 V
4.1.3.73	990 Hz Period	1,009.901 μSec		1,010.301 μSec
4.1.3.74	990 Hz Voltage	0.988 V		1.012 V

CALIBRATION FOR TEST PANEL CD-3800

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Project AN/AQA-7(V)

Paragraph	Description	Recorded Data		
		L.L.	Test Data	U.L.
4.1.3.56	2,400 Hz Voltage	0.988 V		1.012 V
4.1.3.57	2.9838 kHz Period	335.136 µsec		335.150 µsec
4.1.3.58	2.9838 kHz Voltage	3.5 V Pk-Pk		5.25 V Pk-Pk
4.1.3.59	3.3875 kHz Period	295.196 µsec		295.208 µsec
4.1.3.60	3.3875 kHz Voltage	3.5 V Pk-Pk		5.25 V Pk-Pk
4.1.3.61	8.16 kHz Period	122.546 µsec		122.552 µsec
4.1.3.62	8.16 kHz Voltage	3.5 V Pk-Pk		5.25 V Pk-Pk
4.1.3.63	15 kHz Frequency	14.9997 kHz		15.0002 kHz
4.1.3.64	15 kHz Voltage	3.5 V Pk-Pk		5.25 V Pk-Pk
4.1.3.65	26 kHz Frequency	25.9995 kHz		26.0005 kHz
4.1.3.66	26 kHz Voltage	0.988 V		1.012 V
4.1.3.67	38 kHz Frequency	37.9992 kHz		38.0007 kHz
4.1.3.68	38 kHz Voltage	0.988 V		1.012 V
4.1.3.69	2.42 MHz Frequency	2.419950 MHz		2.420050 MHz
4.1.3.70	2.42 MHz Voltage	2.6 V Pk-Pk		5.25 V
4.2.3.1	Omni Noise	591 mV		615 mV
4.2.3.2	Omni Noise	591 mV		615 mV
4.2.3.3	Omni Noise	591 mV		615 mV
4.3.3.1	DEMON Test Carrier Voltage Pk-Pk	-		-
4.3.3.2	Calculated Modulation Ripple Pk-Pk	-		-
4.3.3.4	75 Hz Modulation Ripple Pk-Pk	0.95 x 4.3.3.2		1.05 x 4.3.3.2
4.3.3.6	37.5 Hz Modulation Ripple Pk-Pk	0.95 x 4.3.3.2		1.05 x 4.3.3.2
4.3.3.8	2.5 Hz Modulation Ripple Pk-Pk	0.95 x 4.3.3.2		1.05 x 4.3.3.2
4.4.3.3	Output Ampl. Gain, 0.5. Ch. A	7.960 V		8.040 V
4.4.3.4	Output Ampl. Gain, 0.5. Ch. B	7.960 V		8.040 V
4.4.3.5	Output Ampl. Gain, 0.5. Ch. C	7.960 V		8.040 V
4.4.3.6	Output Ampl. Gain, 0.5. Ch. D	7.960 V		8.040 V
4.4.3.7	Output Ampl. Gain, Gram I	7.960 V		8.040 V
4.4.3.8	Output Ampl. Gain, Gram II	7.960 V		8.040 V
4.4.3.9	Output Ampl. Gain, Gram III	7.960 V		8.040 V
4.4.3.10	Output Ampl. Gain, Gram IV	7.960 V		8.040 V

CALIBRATION FOR TEST PANEL CD-3800

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Serial No. _____

Project AN/AQA-7(V)

Paragraph	Description	Recorded Data		
		L.L.	Test Data	U.L.
4.5.3.1	DIFAR NORM OMNI Signal , 300 Hz	201.7 V		206.6 V
4.5.3.2	TRACK OMNI Signal , 245 Hz	201.7 V		206.6 V
4.5.3.3	TRACK OMNI S/N , 245 Hz	50.6 V		51.8 V
4.5.3.4	DIFAR NORM OMNI, Level 3, 300 Hz	65.4 V		67.0 V
4.5.3.5	DIFAR NORM OMNI, Level 1, 300 Hz	3.27 V		3.35 V
4.5.3.6	DIFAR EXT OMNI, Level 1, 300 Hz	8.23 V		8.43 V
4.5.3.7	DIFAR EXT OMNI, Level 3, 300 Hz	65.4 V		67.0 V
4.5.3.8	ALl LOFAR, EXT, 300 Hz	8.23 V		8.43 V
4.5.3.9	ALl LOFAR, NORM, 300 Hz	3.27 V		3.35 V
4.5.3.10	LOFAR, NORM, 300 Hz	5.20 V		5.32 V
4.5.3.11	LOFAR, EXT, 300 Hz	13.08 V		13.40 V
4.5.3.12	DIFAR NORM OMNI Level 3, 10 Hz	65.4 V		67.0 V
4.5.3.13	TRACK OMNI, 37.5 Hz	65.4 V		67.0 V
4.5.3.14	DIFAR NORM OMNI, Level 3, 37.5 Hz	65.4 V		67.0 V
4.5.3.15	DIFAR NORM OMNI, Level 3, 80 Hz	65.4 V		67.0 V
4.5.3.16	DIFAR EXT OMNI, Level 3, 80 Hz	65.4 V		67.0 V
4.5.3.17	DIFAR NORM OMNI, Level 3, 95 Hz	65.4 V		67.0 V
4.5.3.18	DIFAR NORM OMNI, Level 3, 125 Hz	65.4 V		67.0 V
4.5.3.19	DIFAR NORM OMNI, Level 3, 150 Hz	65.4 V		67.0 V
4.5.3.20	DIFAR NORM OMNI, Level 3, 160 Hz	65.4 V		67.0 V
4.5.3.21	DIFAR NORM OMNI, Level 3, 195 Hz	65.4 V		67.0 V
4.5.3.22	DIFAR EXT OMNI, Level 3, 195 Hz	65.4 V		67.0 V
4.5.3.23	DIFAR NORM OMNI, Level 3, 220 Hz	65.4 V		67.0 V
4.5.3.24	DIFAR NORM OMNI, Level 3, 245 Hz	65.4 V		67.0 V
4.5.3.25	TRACK OMNI, 245 Hz	65.4 V		67.0 V
4.5.3.26	DIFAR NORM OMNI, Level 3, 275 Hz	65.4 V		67.0 V
4.5.3.27	DIFAR EXT OMNI, Level 3, 600 Hz	65.4 V		67.0 V
4.5.3.28	DIFAR EXT OMNI, Level 3, 800 Hz	65.4 V		67.0 V
4.5.3.29	DL OMNI, Level 3, 950 Hz	461 V		473 V
4.5.3.30	DL OMNI, Level 2, 950 Hz	145.8 V		149.3 V
4.5.3.31	DL OMNI, Level 1, 950 Hz	46.1 V		47.3 V
4.5.3.32	DIFAR EXT OMNI, Level 3, 950 Hz	65.4 V		67.0 V

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Project AN/AQA-7(V)

Paragraph	Description	Recorded Data		
		L.L.	Test Data	U.L.
4.5.3.33	DIFAR EXT OMNI, Level 3, 1,200 Hz	65.4 V		67.0 V
4.5.3.34	DIFAR EXT OMNI, Level 3, 1,280 Hz	65.4 V		67.0 V
4.5.3.35	DIFAR EXT OMNI, Level 3, 1,325 Hz	65.4 V		67.0 V
4.5.3.36	DIFAR EXT OMNI, Level 3, 1,700 Hz	65.4 V		67.0 V
4.5.3.37	TRACK OMNI, 2,050 Hz	65.4 V		67.0 V
4.5.3.38	DIFAR EXT OMNI, Level 3, 2,050 Hz	65.4 V		67.0 V
4.5.3.39	DIFAR EXT OMNI, Level 3, 2,400 Hz	65.4 V		67.0 V
4.5.3.40	Remote TRACK OMNI, +20 dB S/N, 1,000 Hz	65.4 V		67.0 V
4.6.3.1	LOFAR, NORM, Noise	380 V		398 V
4.6.3.2	LOFAR, EXT, Noise	380 V		398 V
4.6.3.3	ALl LOFAR, EXT, Noise	380 V		398 V
4.6.3.4	ALl LOFAR, NORM, Noise	380 V		398 V
4.6.3.5	DIFAR NORM OMNI, Noise	380 V		398 V
4.6.3.6	DIFAR EXT OMNI, Noise	380 V		398 V
4.6.3.7	DEMON Noise	380 V		398 V
4.6.3.8	TRACK OMNI, Noise	380 V		398 V
4.6.3.9	DL OMNI, Noise	380 V		398 V
4.7.3.1	NS Baseband Feedthru	-		-
4.7.3.3	EW Baseband Feedthru	-		-
4.7.3.5	EW Reference Input	-		-
4.7.3.10	NS Reference Input	-		-
4.8.3.1	7.5 kHz Pilot Level	1.52 V		1.69 V
4.8.3.3	15 kHz Pilot Level	1.52 V		1.69 V
4.8.3.9	10 Hz, Level 3, Normal DIFAR Level	50.2 mV		52.2 mV
4.8.3.10	37.5 Hz, Level 3, Normal DIFAR Level	50.2 mV		52.2 mV
4.8.3.10	37.5 Hz, Level 3, Normal DIFAR Ratio	0.5750		0.5797
4.8.3.11	80 Hz, Level 3, Normal DIFAR Level	50.2 mV		52.2 mV
4.8.3.11	80 Hz, Level 3, Normal DIFAR Ratio	0.997		1.003
4.8.3.12	95 Hz, Level 3, Normal DIFAR Level	50.2 mV		52.2 mV
4.8.3.13	125 Hz, Level 3, Normal DIFAR Level	50.2 mV		52.2 mV
4.8.3.13	125 Hz, Level 3, Normal DIFAR Ratio	0.5750		0.5797
4.8.3.14	150 Hz, Level 3, Normal DIFAR Level	50.2 mV		52.2 mV
4.8.3.14	150 Hz, Level 3, Normal DIFAR Ratio	0.997		1.003
4.8.3.15	160 Hz, Level 3, Normal DIFAR Level	50.2 mV		52.2 mV

CALIBRATION FOR TEST PANEL CD-3800

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Project AN/AQA-7(V)

Paragraph	Description	Recorded Data		
		L.L.	Test Data	U.L.
4.8.3.16	195 Hz, Level 3, Normal DIFAR Level	50.2 mV		52.2 mV
4.8.3.16	195 Hz, Level 3, Normal DIFAR Ratio	0.5750		0.5797
4.8.3.17	220 Hz, Level 3, Normal DIFAR Level	50.2 mV		52.2 mV
4.8.3.17	220 Hz, Level 3, Normal DIFAR Ratio	0.997		1.003
4.8.3.18	245 Hz, Level 3, Normal DIFAR Level	50.2 mV		52.2 mV
4.8.3.19	275 Hz, Level 3, Normal DIFAR Level	50.2 mV		52.2 mV
4.8.3.19	275 Hz, Level 3, Normal DIFAR Ratio	0.5750		0.5797
4.8.3.20	300 Hz, Level 3, Normal DIFAR Level	50.2 mV		52.2 mV
4.8.3.20	300 Hz, Level 3, Normal DIFAR Ratio	0.997		1.003
4.8.3.23	80 Hz, Level 3, Extended DIFAR Level	50.2 V		52.2 V
4.8.3.24	195 Hz, Level 3, Extended DIFAR Level	50.2 mV		52.2 mV
4.8.3.24	195 Hz, Level 3, Extended DIFAR Ratio	0.5750		0.5797
4.8.3.25	300 Hz, Level 3, Extended DIFAR Level	50.2 mV		52.2 mV
4.8.3.25	300 Hz, Level 3, Extended DIFAR Ratio	0.997		1.003
4.8.3.26	600 Hz, Level 3, Extended DIFAR Level	50.2 mV		52.2 mV
4.8.3.27	800 Hz, Level 3, Extended DIFAR Level	50.2 mV		52.2 mV
4.8.3.27	800 Hz, Level 3, Extended DIFAR Ratio	0.5750		0.5797
4.8.3.28	950 Hz, Level 3, Extended DIFAR Level	50.2 mV		52.2 mV
4.8.3.28	950 Hz, Level 3, Extended DIFAR Ratio	0.997		1.003
4.8.3.29	1,200 Hz, Level 3, Extended DIFAR Level	50.2 mV		52.2 mV
4.8.3.30	1,280 Hz, Level 3, Extended DIFAR Level	50.2 mV		52.2 mV
4.8.3.30	1,280 Hz, Level 3, Extended DIFAR Ratio	0.5750		0.5797
4.8.3.31	1,325 Hz, Level 3, Extended DIFAR Level	50.2 mV		52.2 mV
4.8.3.31	1,325 Hz, Level 3, Extended DIFAR Ratio	0.997		1.003
4.8.3.32	1,700 Hz, Level 3, Extended DIFAR Level	50.2 mV		52.2 mV
4.8.3.33	2,050 Hz, Level 3, Extended DIFAR Level	50.2 mV		52.2 mV
4.8.3.33	2,050 Hz, Level 3, Extended DIFAR Ratio	0.5750		0.5797
4.8.3.34	2,400 Hz, Level 3, Extended DIFAR Level	50.2 mV		52.2 mV
4.8.3.34	2,400 Hz, Level 3, Extended DIFAR Ratio	0.997		1.003
4.8.3.37	Normal DIFAR, Level 1, Signal Level	2.51 mV		2.61 mV

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Project AN/AQA-7(V)

Paragraph	Description	Recorded Data		
		L.L.	Test Data	U.L.
4.8.3.38	Normal DIFAR, Level 1, EW Signal Level	-		-
4.8.3.39	Normal DIFAR, Level 1, NS Signal Level	0.995 x 4.8.3.38		1.005 x 4.8.3.38
4.8.3.40	Ext DIFAR, Level 1, Signal Level	6.32 mV		6.58 mV
4.8.3.41	Ext DIFAR, Level 1, EW Signal Level	-		-
4.8.3.42	Ext DIFAR, Level 1, NS Signal Level	0.995 x 4.8.3.41		1.005 x 4.8.3.41
4.8.3.50	DL, Level 3, 0 deg Signal Level	355 mV		369 mV
4.8.3.51	DL, Level 3, 90 deg Signal Level	355 mV		369 mV
4.8.3.52	DL, Level 3, 45 deg Signal Level	355 mV		369 mV
4.8.3.52	DL, Level 3, 45 deg Ratio	0.997		1.003
4.8.3.53	DL, Level 3, 135 deg Signal Level	355 mV		369 mV
4.8.3.53	DL, Level 3, 135 deg Ratio	0.997		1.003
4.8.3.54	DL, Level 3, 315 deg Signal Level	355 mV		369 mV
4.8.3.54	DL, Level 3, 315 deg Level Ratio	0.997		1.003
4.9.3.1	TRACK Potentiometer Dirve Balance	0.999		1.001
4.9.3.4	TRACK Intercardinal Ratio	0.995		1.005
4.9.3.4	TRACK Intercardinal Signal Level	50.2 mV		52.2 mV
4.9.3.6	Remote Track 45 deg Ratio	0.995		1.005
4.9.3.6	Remote Track 45 deg Signal Level	50.2 mV		52.2 mV
4.10.3.2	DIFAR, Normal NS Noise	295 mV		309 mV
4.10.3.3	DIFAR, Extended NS Noise	295 mV		309 mV
4.10.3.4	TRACK NS Noise	295 mV		309 mV
4.10.3.5	DL NS Noise	295 mV		309 mV
4.10.3.6	DIFAR Extended EW Noise	295 mV		309 mV
4.10.3.7	DIFAR Normal EW Noise	295 mV		309 mV
4.10.3.8	TRACK EW Noise	295 mV		309 mV
4.10.3.9	DL EW Noise	295 mV		309 mV
4.11.3.1	BITE S+N Output Ref.	-		-
4.11.3.3	BITE S+N Output	0.995 x 4.11.3.1		1.005 x 4.11.3.1
4.11.3.6	Best Null, NS Channel	-		-
4.11.3.9	BITE DL NS Signal	-		-
4.11.3.11	BITE DL EW Signal	0.995 x 4.11.3.9		1.005 x 4.11.3.9
4.11.3.13	ASSG Amplifier Input Reference	-		-
4.11.3.15	ASSG Amplifier Output	0.99 x 4.11.3.13		1.01 x 4.11.3.13

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Project AN/AQA-7(V)

Paragraph	Description	Recorded Data		
		L.L.	Test Data	U.L.
4.12.3.2	Active, Noise Only, Range B	0.98mV		1.02mV
4.12.3.3	Active, Noise Only, Range A	0.98mV		1.02mV
4.12.3.4	Q47 Noise	37.2 mV		38.8 mV
4.12.3.5	Q50, CW, 0.1, Noise	37.2 mV		38.8 mV
4.12.3.6	Q50, CW, 0.5, Noise	70.2 mV		73.2 mV
4.12.3.7	Q50, CW, 1.0, Noise	98 mV		102 mV
4.12.3.8	Q50, FM Noise	98 mV		102 mV
4.12.3.15	615 Hz Target	82.7 mV		86.0 mV
4.12.3.16	603 Hz Target	82.7 mV		86.0 mV
4.12.3.17	600 Hz Target	82.7 mV		86.0 mV
4.12.3.18	Zero Doppler A	147 mV		152 mV
4.12.3.19	Q47 Ping	0.98 V		1.02 V
4.12.3.20	1,325 Hz Target	14.7 mV		15.2 mV
4.12.3.21	1,000 Hz, Level 1 Target	14.7 mV		15.2 mV
4.12.3.22	1,000 Hz, Level 3 Target	82.7 mV		86.0 mV
4.12.3.23	800 Hz Target	37.1 mV		38.5 mV
4.12.3.24	Q50, FM, Level 1	20.7 mV		21.5 mV
4.12.3.25	Q50, FM, Level 3	117 mV		121 mV